## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

## DEVICE ORDER INFORMATION

| | | |
|---|---|---|
| SCT2632STE | 2632 | ESOP-8 |

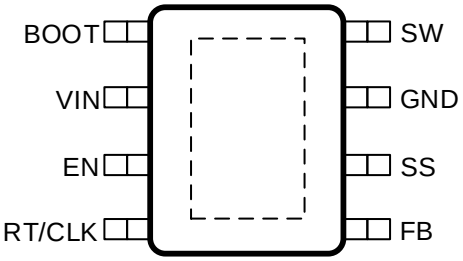
1) For Tape & Reel, Add Suffix R (e.g. SCT2632STER)

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

| | | | |
|---|---|---|---|
| VIN, EN | -0.3 | 65 | V |
| BOOT | -0.3 | 72 | V |
| SW | -1 | 65 | V |
| BOOT-SW | -0.3 | | |

## PIN CONFIGURATION

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| | |
|---|---|
| 7 | Ground |
| 8 | Regulator switching output. Connect SW to an external power inductor |
| 9 | Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance. |

## OPERATING CONDITIONS

emperature range unless otherwise noted

| | | | |
|---|---|---|---|
| ut voltage range | 4.5 | 60 | V |
| put voltage range | 0.8 | 57 | V |
| erating junction temperature | -40 | 150 | ÁC |

| | | | | |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1) | -2 | +2 | kV |
| | Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2) | -0.5 | +0.5 | kV |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## THERMAL INFORMATION

| | | | |
|---|---|---|---|
| | Junction-to-ambient thermal resistance (standard board) | 42 | ÁC/W |
| | Junction-to-top characterization parameter | 5.9 | |

## ELECTRICAL CHARACTERISTICS

C, typical value is tested under 25ÁC.

| | | | | | |
|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage | | 4.2 | 60 | V |
| $V_{IN_UVLO}$ | Input UVLO Threshold<br>Hysteresis | $V_{IN}$ rising | 3.5<br>400 | | V<br>mV |
| $I_{SHDN}$ | Shutdown current from VIN pin | EN=0, no load | 2 | 5 | εA |
| $I_Q$ | Quiescent current from VIN pin | EN floating, no load, non-switching, BOOT-SW=5V, $R_{RT}$=200 kÝ | 100 | | εA |
| $R_{DSON_H}$ | High-side MOSFET on-resistance | $V_{BOOT}$-$V_{SW}$=5V | 220 | | mÝ |
| V | Reference voltage of FB | | 0.792 | 0.8 | |


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| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | |
| $I_{LIM_HS}$ | High-side power MOSFET peak current limit threshold | | 4.6 | 5.2 | 5.8 | A |
| | | | | | | |
| $V_{EN_H}$ | Enable high threshold | | | 1.2 | | V |
| $V_{EN_L}$ | Enable low threshold | | | 1.05 | | V |
| $I_{EN_L}$ | Enable pin pull-up current | EN=1V | | 1 | | εA |
| $I_{EN_H}$ | Enable pin pull-up current | EN=1.5V | | 4 | | uA |
| $I_{SS}$ | SS pin current | | | 2.6 | | uA |
| | | | | | | |
| $F_{RANGE_RT}$ | Frequency range using RT mode | | 100 | | 1200 | kHz |
| $F_{SW}$ | Switching frequency | $R_{RT}$=200 kÝ(1%) | 450 | 500 | 550 | kHz |


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## TYPICAL CHARACTERISTICS

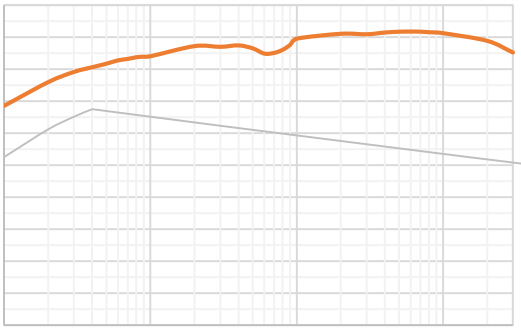

Figure 2. Efficiency vs Load Current, Vout=5V

Figure 3. Efficiency vs Load Current, Vin=24V

Figure 4. Load Regulation, Vin=24V, Vout=5V

Figure 5. Current Limit VS Temperature

Figure 6. Switching Frequency VS Temperature

Figure 7. Switching Frequency vs RT Resistor


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## FUNCTIONAL BLOCK DIAGRAM

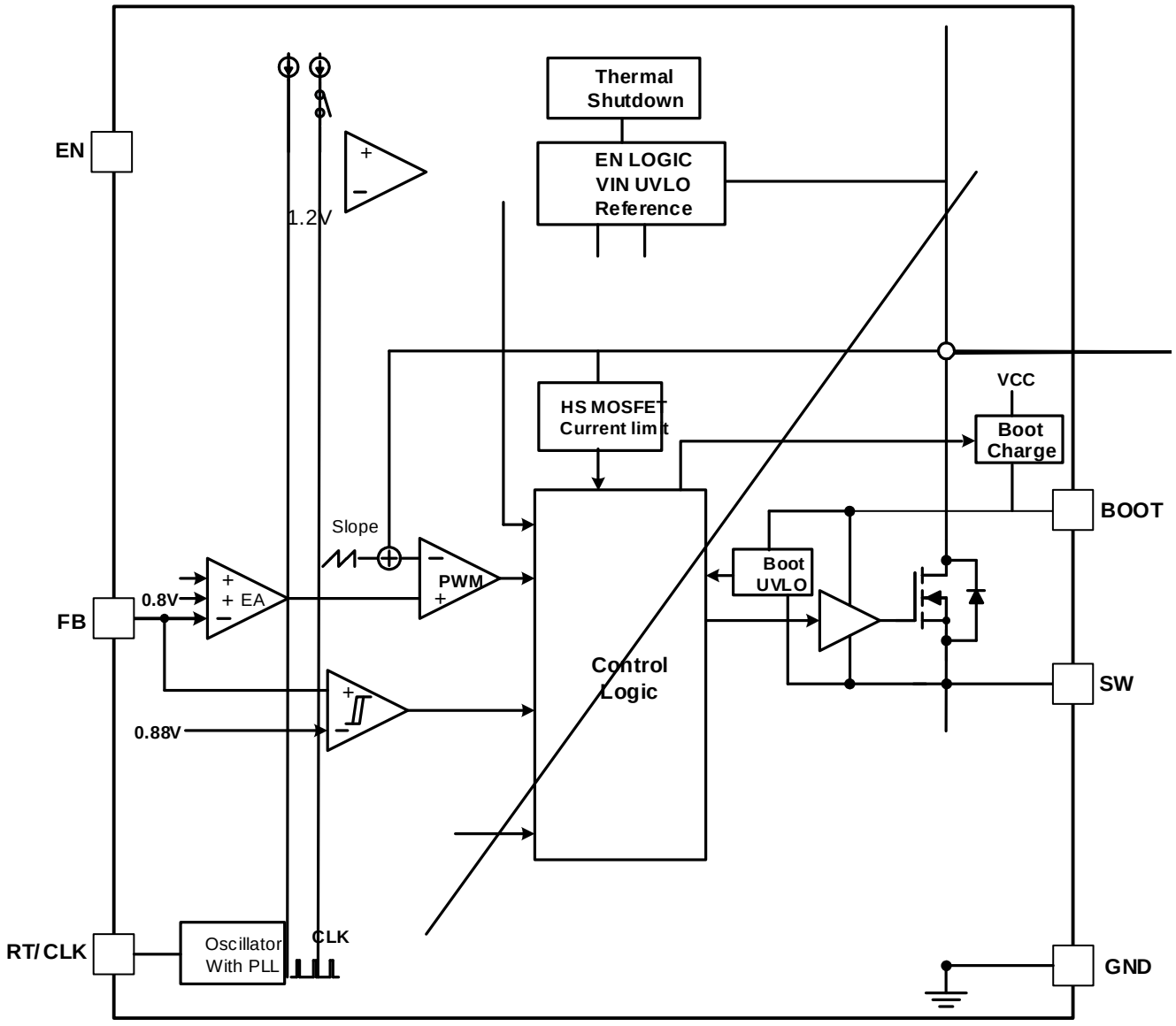


Figure 8. Functional Block Diagram

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## OPERATION

The SCT2632 is a 4.2V-60V input, 3A output, buck converter with integrated 220mq Rdson high-side power MOSFET. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is programmable from 100kHz to 1.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external componentsô sizes. The SCT2632 features adjustable soft-start to avoid large inrush current. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 100uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2632 has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2632 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting, output hard short protection and thermal shutdown protection.

The SCT2632 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off.

The error amplifier servos the COMP node by comparing the voltage of the FB pin with an internal 0.8V mU

(1)

(2)

where

$V_{rise}$ is rising threshold of Vin UVLO

$V_{fall}$ is falling threshold of Vin UVLO

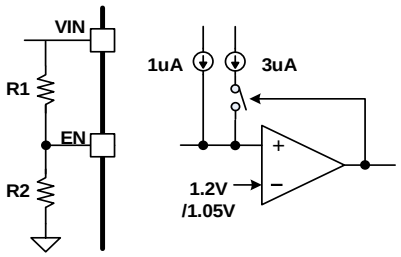


Figure 9. System UVLO by enable divide

The SCT2632 regulates the internal reference voltage at 0.8V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

(3)

where

$R_{FB_TOP}$ is the resistor connecting the output to the FB pin.

$R_{FB_BOT}$ is the resistor connecting the FB pin to the ground.

The SCT2632 features programmable soft-start time to prevent inrush current during start-up stage. The soft-start time can be programmed easily by connecting a soft-start capacitor $C_{ss}$ ($C_{ss}$ is the C6 on Figure 11) from SS pin to ground.

The SS pin sources an internal 3ÕA current charging the external soft-start capacitor $C_{ss}$ when the EN pin exceeds turn-on threshold. The device adopts the lower voltage between the internal voltage reference 0.8V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 0.8V.

The soft-start capacitor value can be calculated going with following equation 4. Attention should be taken here that the programmed soft-start time should be larger than 4ms.

(4)

Where:

$C_{SS}$ is the soft-start capacitor connected from SS pin to the ground

$t_{ss}$ is the soft-start time

The switching frequency of the SCT2632 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 1.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 5 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

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where, fsw is switching clock frequency

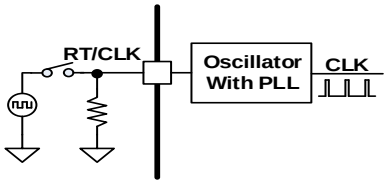


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100KHz to 1.2MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 εF

The UVLO of high-side MOSFET gate driver has rising threshold of 2.5V and hysteresis of 230mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.27V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converterôs operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2632 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.5V. When the voltage from BOOT to SW drops below 2.27V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.5V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2632 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

The SCT2632 implements over current protection with fold back current limit. The SCT2632 cycle-by-cycle limits high-side MOSFET peak current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously.

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The SCT2632 implements frequency foldback to protect the converter in unexpected overload or output hard short condition at higher switching frequencies and input voltages. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The SCT2632 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum on-time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off-time. The frequency foldback effectively increases the off-time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 6 calculates the maximum switching frequency at which the inductor current remains under control when $V_{OUT}$ is forced to $V_{OUT_SHORT}$. The selected operating frequency must not exceed the calculated value.

(6)

where

: Limited average current

: Inductor DC resistance

_ : Maximum input voltage

_ : Output voltage during short

: Diode voltage drop

: Integrated high side FET on resistance

_ : Controllable minimum on time

: Frequency divide equals (1,2,4 or 8)

The SCT2632 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

The SCT2632 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172 degrees, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160 degrees, the device restarts with soft start phase.

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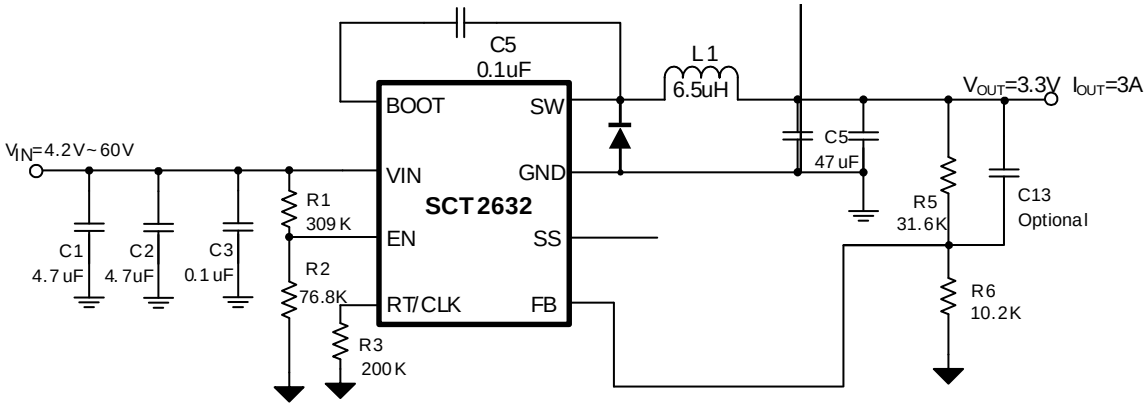
## APPLICATION INFORMATION




| | |
|---|---|
| Input Voltage | 24V Normal 4.2V to 60V |
| Output Voltage | 3.3V |
| Maximum Output Current | 3A |
| Switching Frequency | 500 KHz |
| Output voltage ripple (peak to peak) | 16.5mV |
| Transient Response 0.75A to 2.25A load step | æVout = 160mV |
| Start Input Voltage (rising VIN) | 5.73V |
| Stop Input Volta 0 g IN) | |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The peak-to-peak ripple current in the inductor $I_{LPP}$ can be calculated as in Equation 11.

(11)

Where

$I_{LPP}$ is the inductor peak-to-peak current
L is the inductance of inductor
$f_{SW}$ is the switching frequency
$V_{OUT}$ is the output voltage
$V_{IN}$ is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 12 to calculate the inductance value.

(12)

Where

$L_{MIN}$ is the minimum inductance required
$f_{sw}$ is the switching frequency
$V_{OUT}$ is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of $I_{LPP}$ to $I_{OUT}$

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, $I_{LPEAK}$ and $I_{LRMS}$ can be calculated as in equation 13 and equation 14.

(13)

(14)

Where

$I_{LPEAK}$ is the inductor peak current
$I_{OUT}$ is the DC load current
$I_{LPP}$ is the inductor peak-to-peak current
$I_{LRMS}$ is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5.2A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5.2A. Because of the maximum $I_{LPEAK}$ limited by device, the maximum output current that the SCT2632 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

The SCT2632 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than


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the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2632.

For the example design, the B360B-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B360B-13-F is 0.7 volts at 3 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B360B-13-F diode has a junction capacitance of 200 pF. Using Equation 15, the total loss in the diode at the maximum input voltage is 1W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

(15)

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 16.

(16)

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

(17)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 18 and the maximum input voltage ripple occurs at 50% duty cycle.

(18)

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For this example, two 4.7εF, X7R ceramic capacitors rated for 100 V in parallel are used. And add 0.1με F ceramic capacitor in parallel a╬ frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1εF ceramic capacito strap Capacito d acitŃ a



@ 0 é«Ì-à

Vin=24V, Vout=3.3V, unless otherwise noted

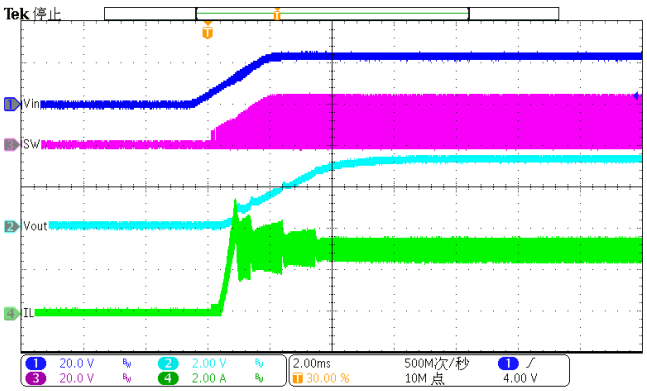


Figure 12. Power up(Iload=3A)

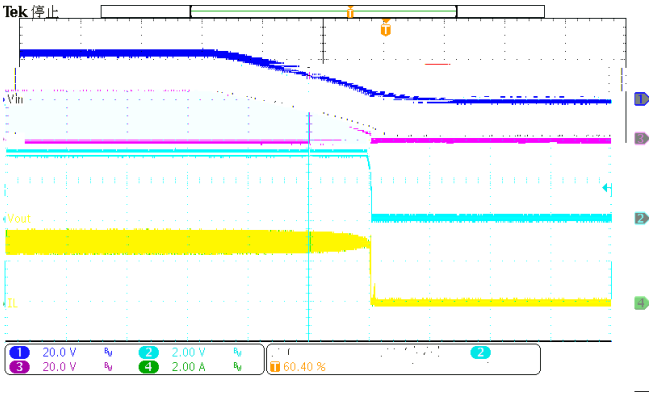


Figure 13. Power down(Iload=3A)

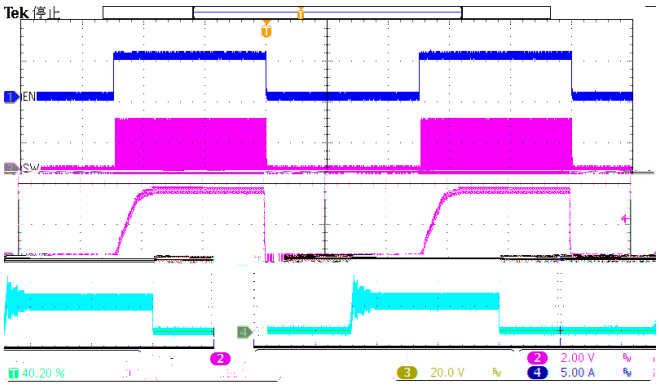


Figure 14.EN toggle (Iload= A)

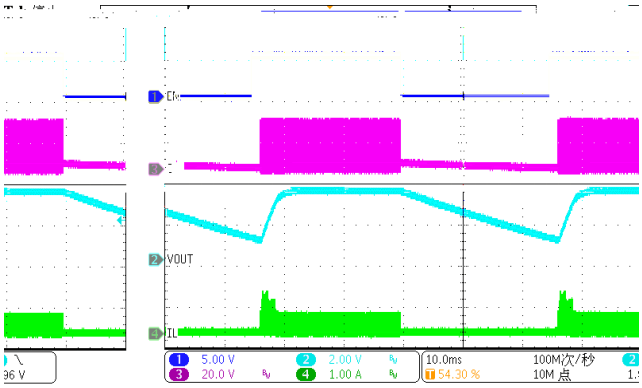


Figure 15. EN toggle (Iload=20mA)

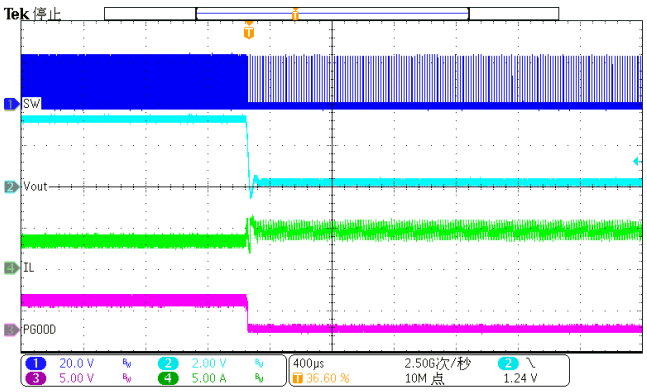


Figure 16. Over Current Protection(3A to hard short)

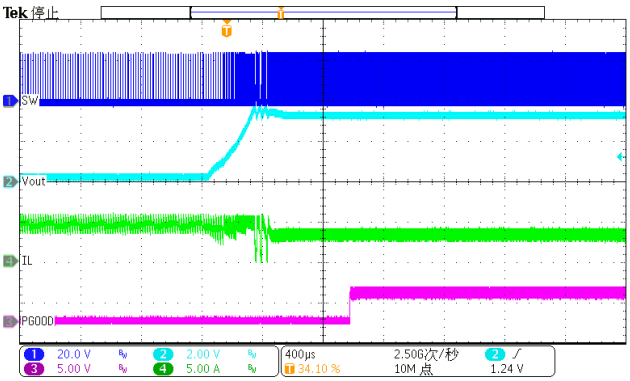


Figure 17. Over Current Release (hard short to 3A)

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Vin=24V, Vout=3.3V, unless otherwise noted

Figure 18. Load Transient (0.3A-2.7A h ' t

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Proper PCB layout is a critical for SCT2632ûs stable and efficient operation.

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## PACKAGE INFORMATION

SOP8/PP(95x130) Package Outline Dimensions

| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |


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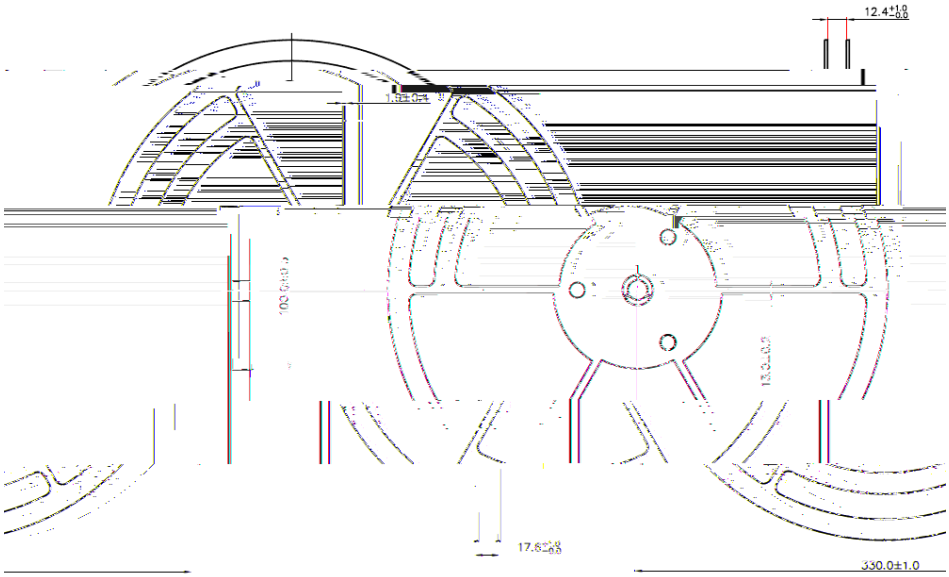
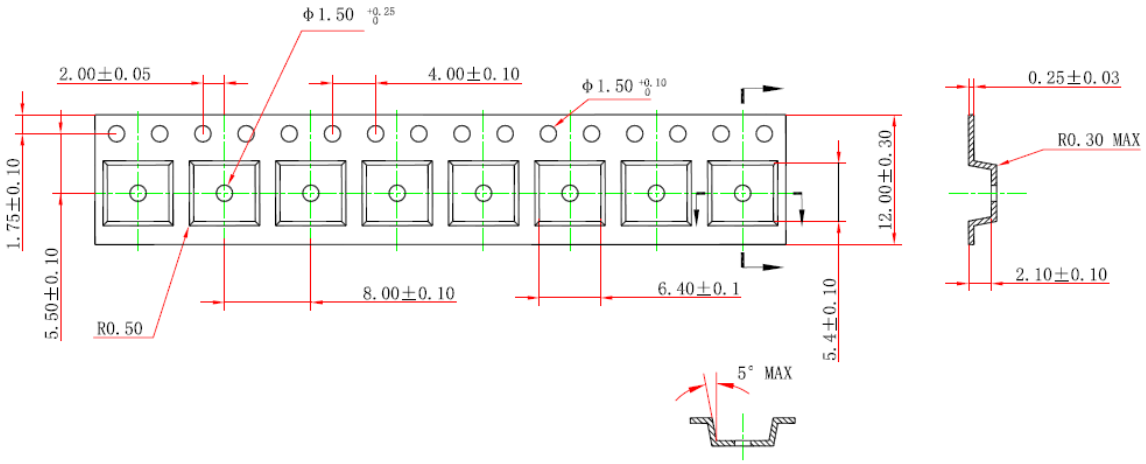
## TAPE AND REEL INFORMATION

| Orderable Device | Package Type | Pins | SPQ |
|---|---|---|---|
| SCT2632STER | ESOP | 8 | 4000 |

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