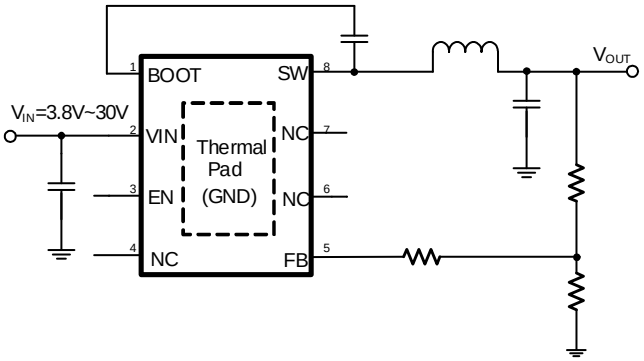
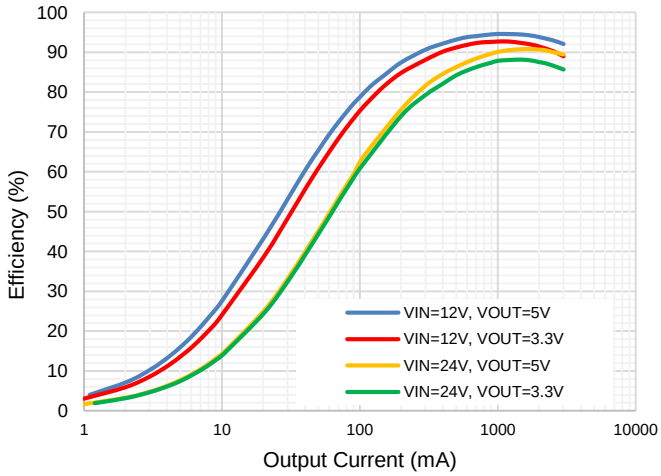
- 3.8V-30V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 85mΩ R_{dson} High Side MOSFET and 58mΩ R_{dson} Low Side MOSFET
- 400kHz Switching Frequency
- Force Pulse Width Modulation (FPWM) Mode
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in ESOP-8 Package

The SCT9339 is 3A synchronous buck converters with up to 30V wide input voltage range, which fully integrates an 85mΩ high-side MOSFET and a 58mΩ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9339 adopts peak current mode control with the integrated compensation network, which makes SCT9339 easily to be used by minimizing the off-chip component count. The SCT9339 supports Force Pulse Width Modulation (FPWM) Mode to achieve the small output ripple at light load condition.

The SCT9339 offers output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available ESOP-8 package.

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display





NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

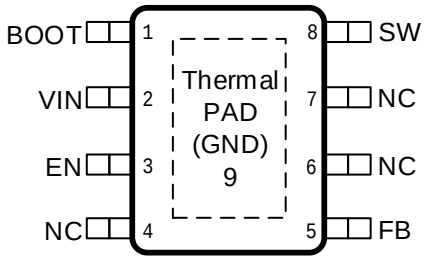
Revision 1.5: Upgrade to 30V, add high low limit in EC table

N PRLSK CP	N AI ECK PI GE	N AI EC BG AP GRML
SCT9339STE	9339	8-Lead Plastic ESOP

1 For Tape & Reel, Add Suffix R (e.g. SCT9339STER).

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
BST-SW	-0.3	6	V
FB	-0.3	5.5	V
Operating junction temperature(2)	-40	125	C
Storage temperature T_{STG}	-65	150	C



8-Lead Plastic E-SOP

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

L KC	LM,	NG DSL ARGML
BOOT	1	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
VIN	2	Power supply input. Must be locally bypassed.
EN	3	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
FB	5	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
NC	4, 6,7	Not connected.
SW	8	Switching node of the buck converter.

Thermal Pad	9	GND and Heat dissipation path of die. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Over operating free-air temperature range unless otherwise noted

NPKCRCP	BCDGLGRGML	KGL	KV	SLGR
V_{IN}	Input voltage range	3.8	30	V
T_J	Operating junction temperature	-40	125	°C

NPKCRCP	BCDGLGRGML	KGL	KV	SLGR
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

NPKCRCP	RFCPK KCRPGA	CMN	SLGR
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45.8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT9339 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT9339. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

KM	NPKCRCP	RCRAMLBGRGML	KGL RNKV	SLGR
N M				
V_{IN}	Operating input voltage		3.8 30	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising	3.5 420	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V	1 3	uA
I_Q	Quiescent current	EN=floating, No load, No switching. BST-SW=5V	250	uA
C U K				
V_{EN_H}	Enable high threshold		1.18	V
V_{EN_L}	Enable low threshold		1.1	V
I_{EN}	Enable pin input current	EN=1V	1.5	uA
I_{EN_HYS}	Enable pin hysteresis current	EN=1.5V	4	uA
N KM DCR				
R_{DSON_H}	High side FET on-resistance		85	mΩ

K M	N P K CRCP	RC R AMLBGRGML	KG R N K V	SLGR
R_{DSON_L}	Low side FET on-resistance			

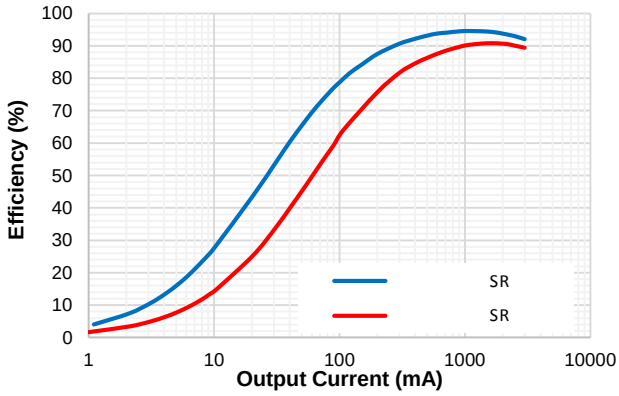


Figure 1. Efficiency vs Load Current, Vout=5V

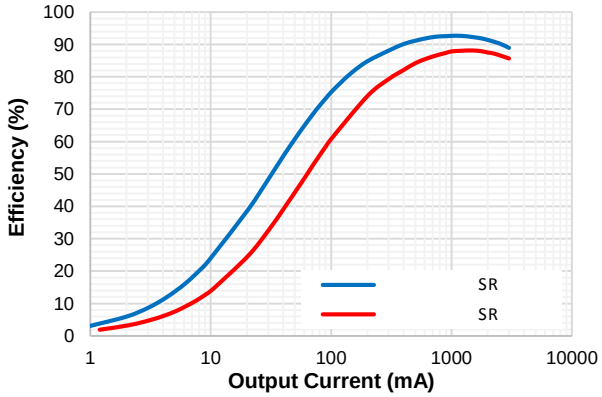


Figure 2. Efficiency vs Load Current, Vin=12V

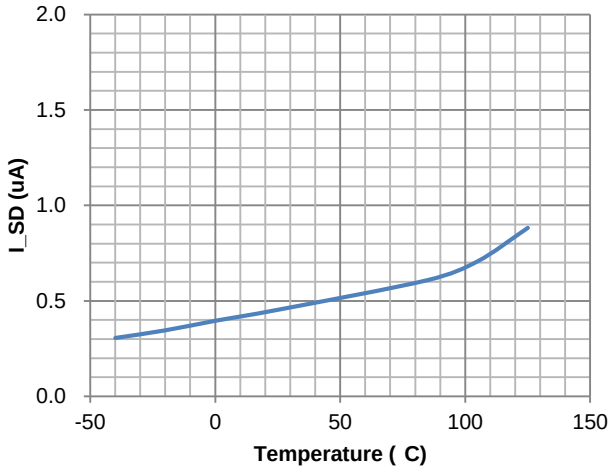


Figure 3. Shut-down Current vs Temperature

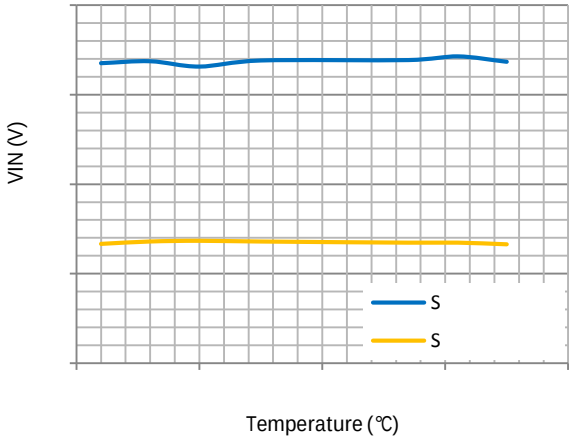


Figure 4. VIN UVLO vs Temperature

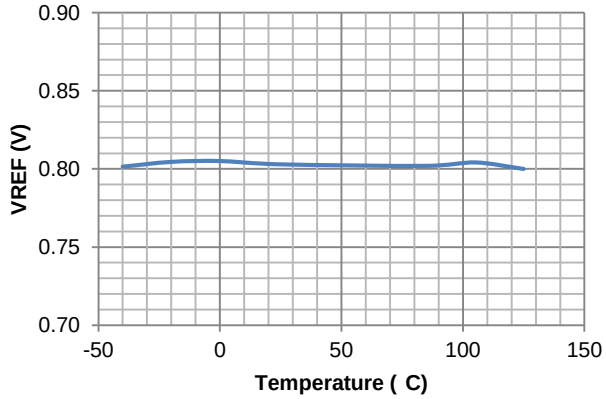


Figure 5. Reference Voltage vs Temperature

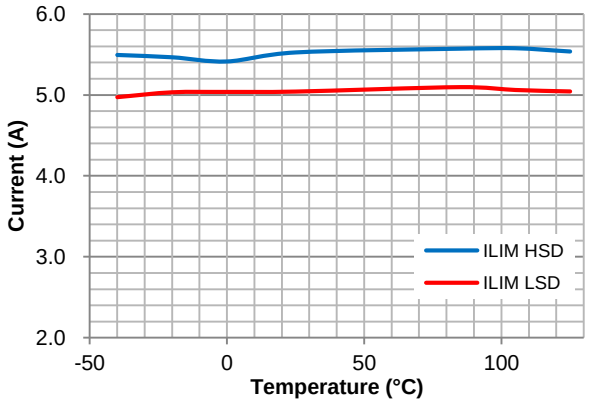


Figure 6. Peak Current Limit vs Temperature

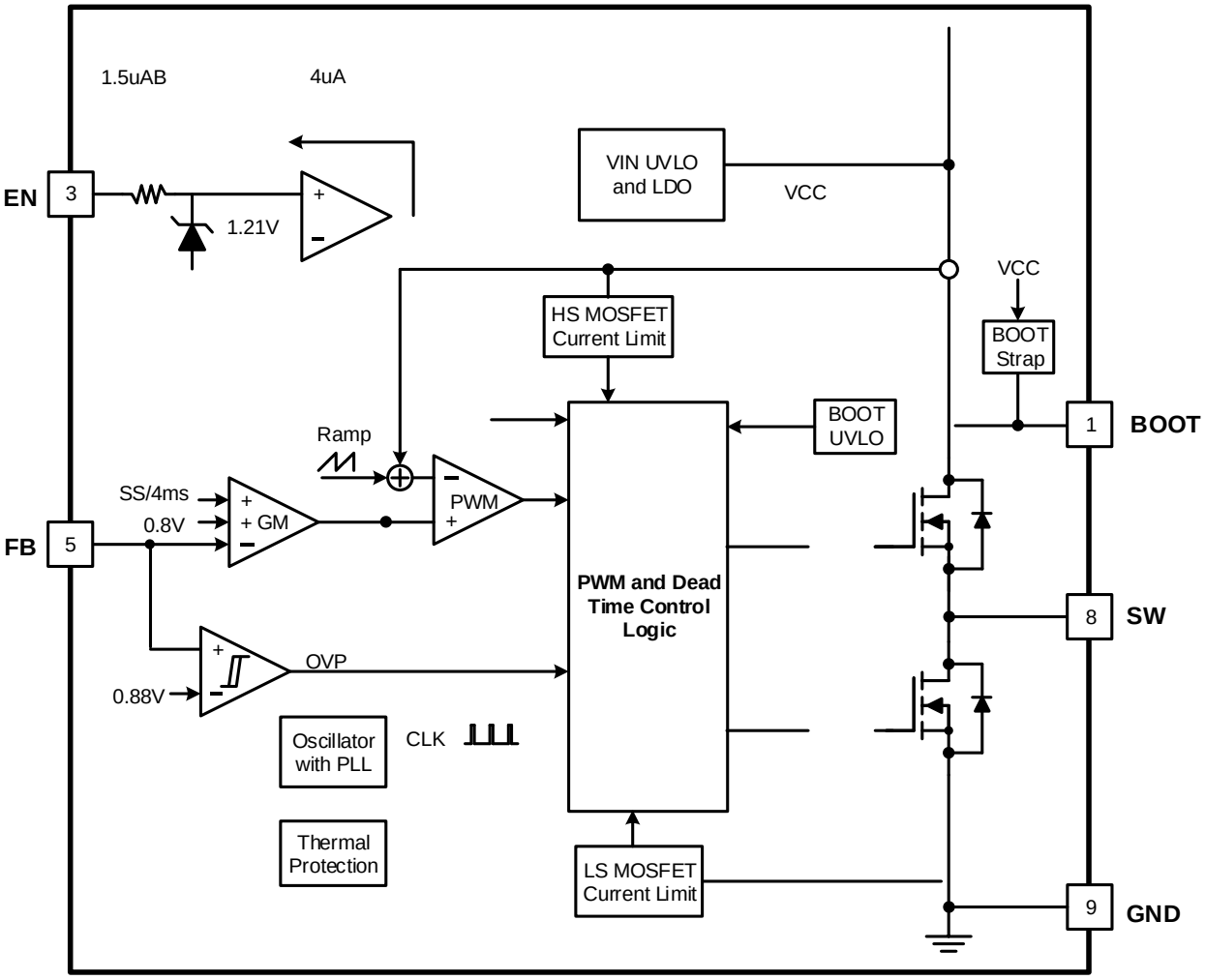


Figure 7. Functional Block Diagram

M

The SCT9339 device is 3.8V-30V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 400kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT9339 footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

To provide the lower output ripple in light load condition, the SCT9339 offers adjustable switching frequency and works at the Force Pulse Width Modulation (FPWM) mode.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9339 device also features full protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

TG N

The SCT9339 is designed to operate from an input voltage supply range between 3.8V to 30V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

S T ST M

The SCT9339 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.08V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

C

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9339 enables all functions and the device starts soft-start phase. The SCT9339 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a k EN or N" EN or N

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

D N U K DNU K U K

To provide the lower output ripple in light load condition, the SCT9339 offers the fixed switching frequency which set by the Rt resistor and works at the Force Pulse Width Modulation (FPWM) mode.

T P

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9339

AR

R

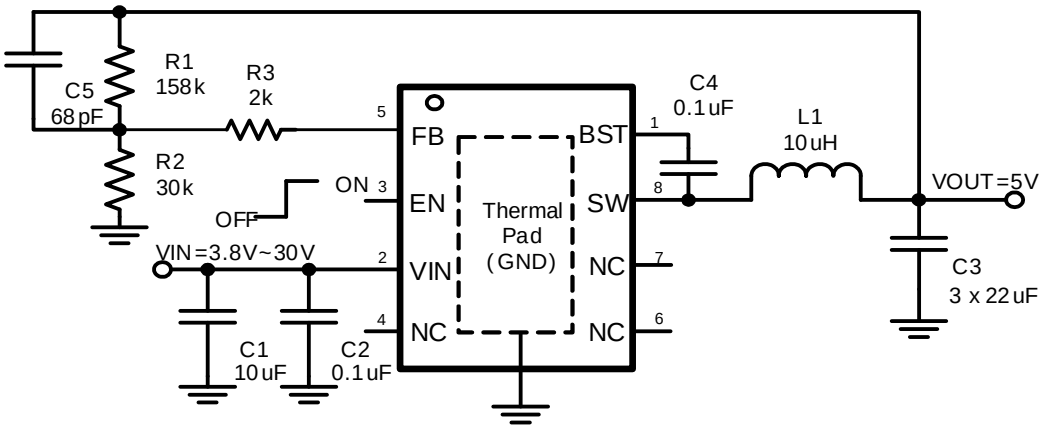


Figure 10. 24V Input, 5V/3A Output

B N

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	400kHz

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

M A

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-

The SCT9339 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

(10)

M D P B

The SCT9339 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 10. Use equation (11) to calculate the resistor divider values.

(11)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

U

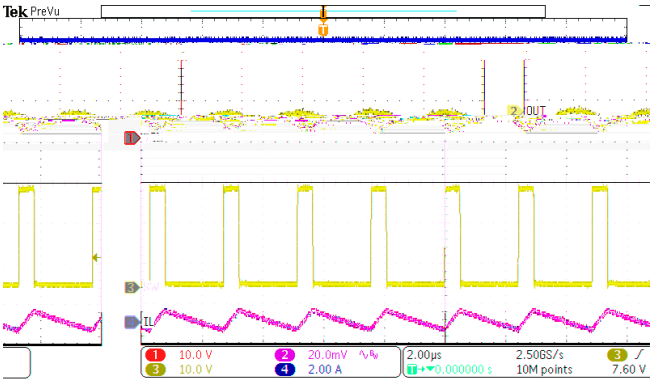


Figure 11.SW Node Waveform and Output Ripple
VIN=24V, IOUT=10mA

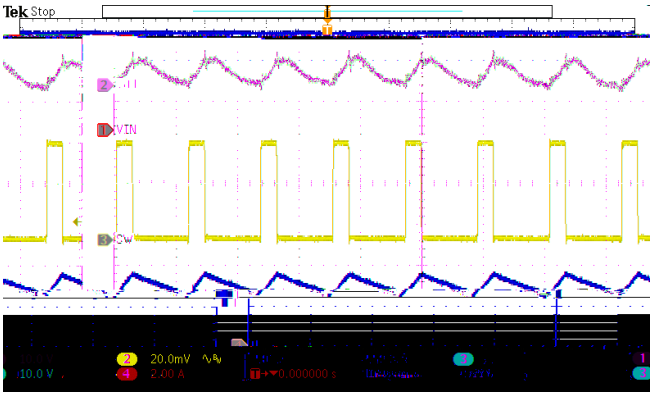


Figure 12.SW Node Waveform and Output Ripple
VIN=24V, IOUT=3A

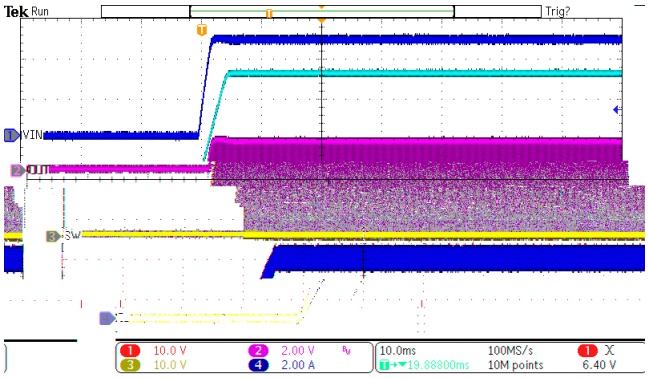


Figure 13. Power Up
VIN=24V, VOUT=5V, IOUT=3A

Figure 14. Power Down
VIN=24V, VOUT=5V, IOUT=3A

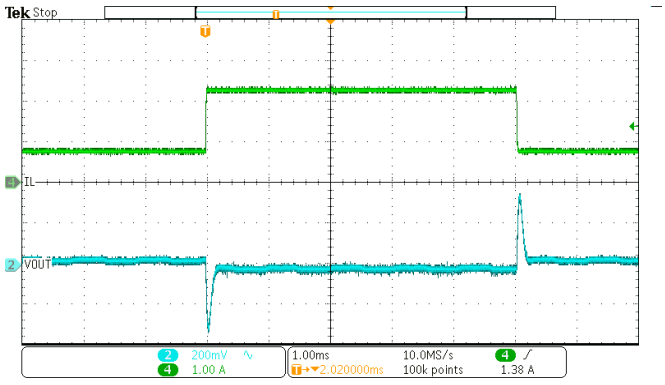


Figure 15. Load Transient
VOUT=5V, IOUT=0.75A to 2.25 A, SR=250mA/us

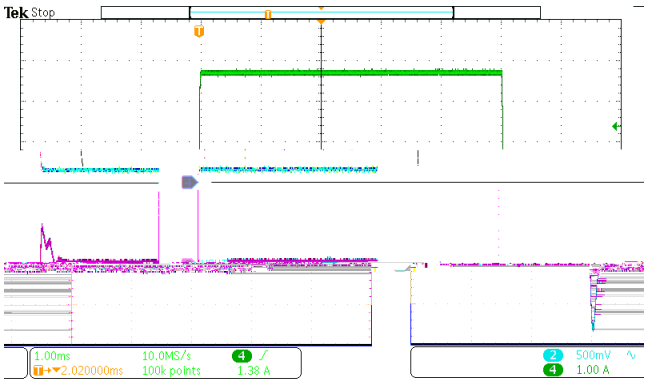


Figure 16. Load Transient
VOUT=5V, IOUT=0.3A to 2.7A, SR=250mA/us

E

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 17 is the recommended PCB layout of SCT9339.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

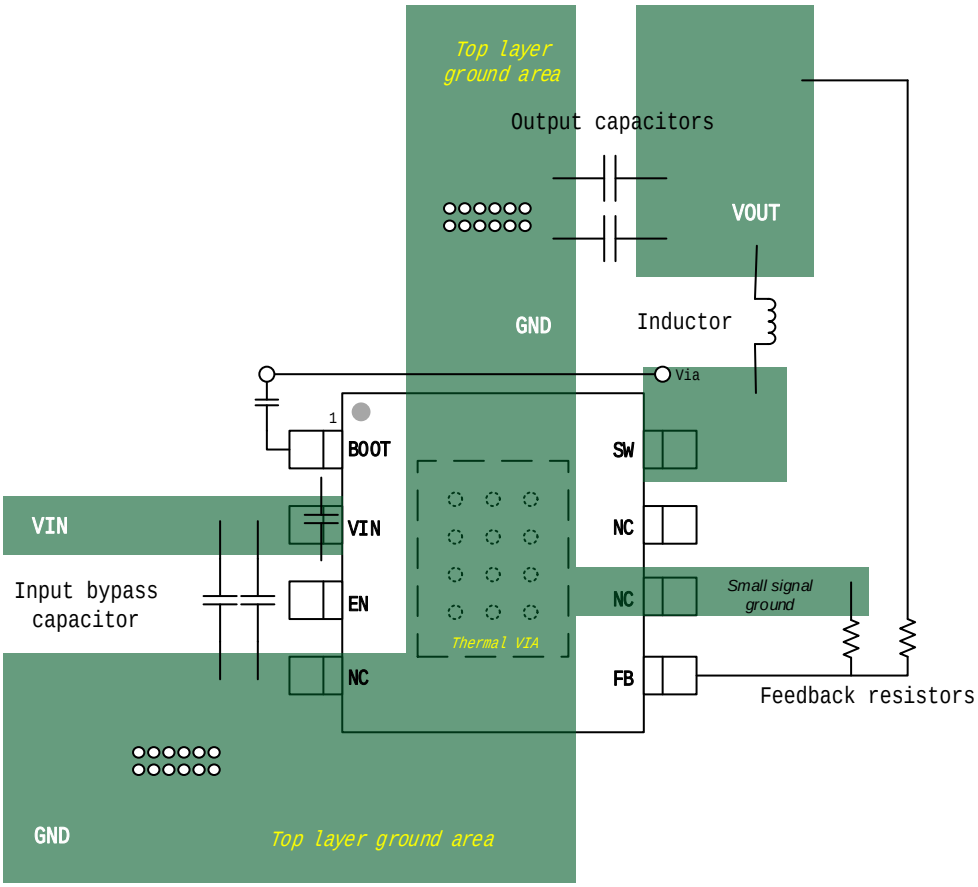
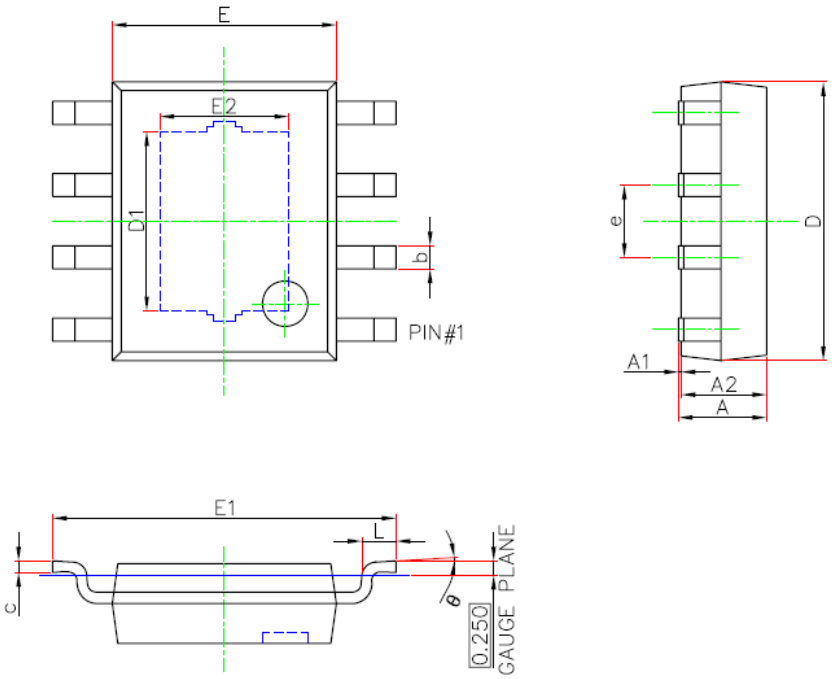


Figure 17. PCB Layout Example

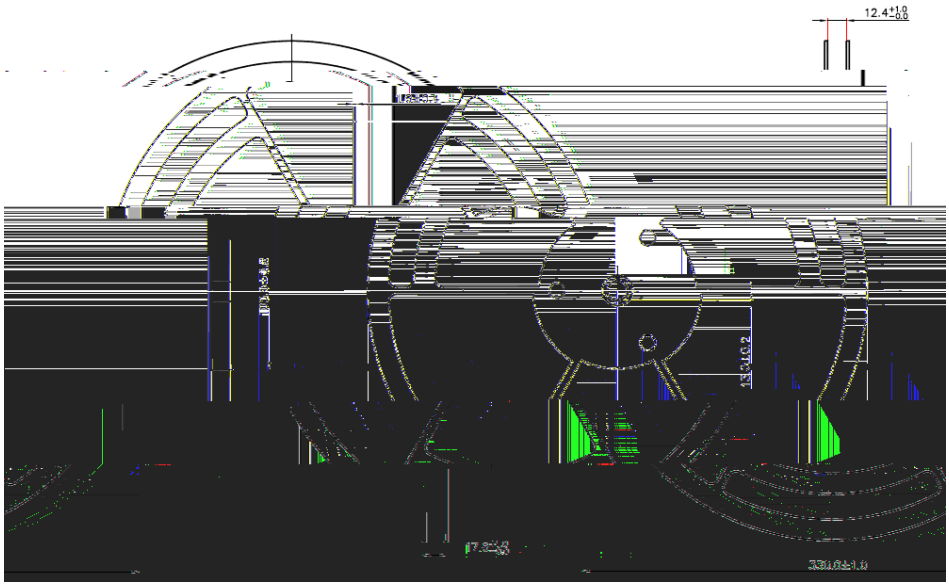


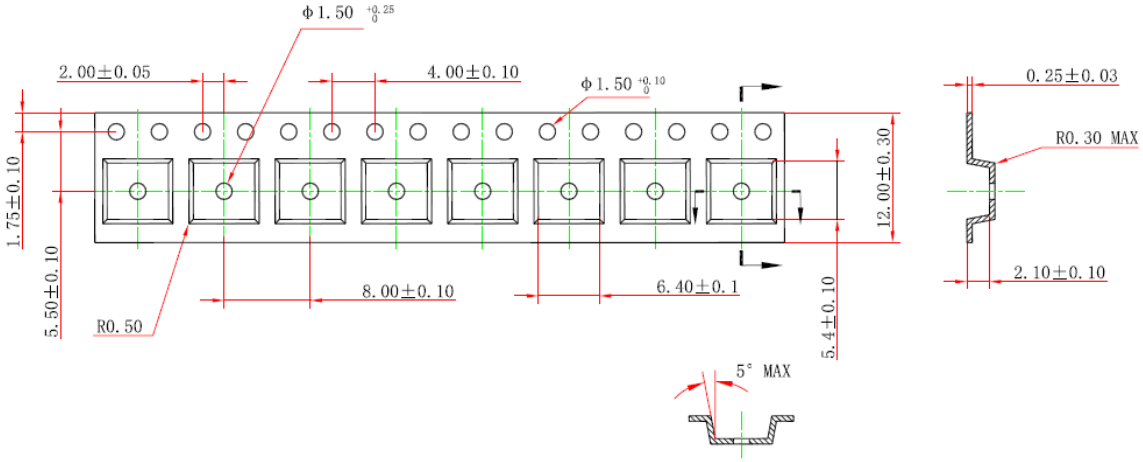
ESOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

LMRC8

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.




Φ1.50 +0.25 0
2.00±0.05
4.00±0.10
Φ1.50 +0.10 0
0.25±0.03
R0.30 MAX
1.75±0.10
5.50±0.10
12.00±0.30
8.00±0.10
6.40±0.1
2.10±0.10
R0.50
5.4±0.10
5° MAX