- Wide Input Voltage Range: 3.1V-50V
- Low Shutdown Current 3.9uA
- Low Quiescent Operating Current: 415uA
- +/- 1.5% Feedback Reference Voltage
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- External Frequency Synchronic
- External Compensation
- Pulse Skipping Mode
- Supports additional Slope Compensation
- 14ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjustable Under-voltage Lockout
  - Thermal Shutdown Protection:165°C
- MSOP-10L(3mm*3mm)

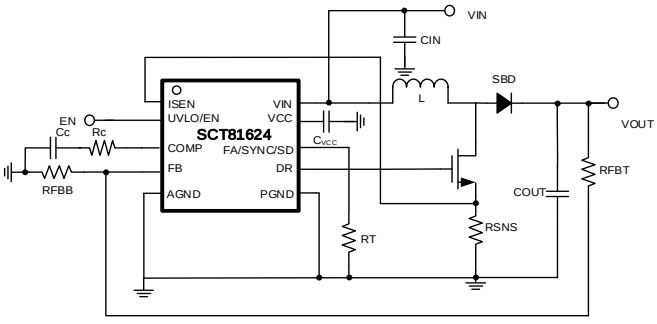
The SCT81624 device is a wide input, non-synchronous boost controller. The device can be used in Boost, SEPIC and Flyback converters.

The switching frequency of the SCT81624 device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

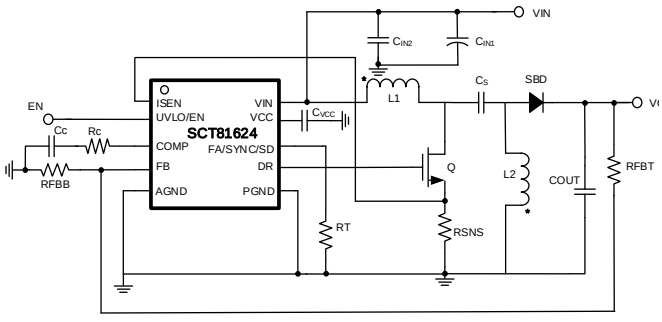
The SCT81624 device has built-in protection features such as thermal shutdown, over-current protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.9 µA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-10L(3mm*3mm) Package.

- Multi-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application



BOOST



SEPIC

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

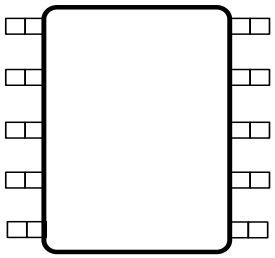
Revision 1.0: Released to Market

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT81624MRD	1624	10-Lead 3mm×3mm Plastic MSOP

1) For Tape & Reel, Add Suffix R (e.g. SCT81624MRDR)

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, UVLO_EN	-0.3	62	V
VCC, DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	C
Storage temperature T_{STG}	-65	150	C



Top View: 10-Lead Plastic MSOP 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

NAME	NO.	DESCRIPTION
DR	8	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
VCC	9	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
VIN	10	Power supply input pin

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.1	50	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

PARAMETER	THERMAL METRIC	MSOP-10	UNIT
R	Junction to ambient thermal resistance(1)	142.3	°C/W
R (top)	Junction to case (top) thermal resistance(1)	64.6	
R B	Junction to board thermal resistance(1)	97.3	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81624 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81624. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.1		50	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.8 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V or V_{UVLO_EN}=0		3.9	8	uA
I_Q	Quiescent current from VIN	no load, no switching, V_{FB}=2V		415		uA
I_{SUPPLY}(1)	Supply Current	$R_{FA/SYNC/SD}$ switching, no load and without external MOSFET		2		mA
VCC Power						
V_{CC}	Internal linear regulator	VIN>7V		6.1		V
V_{CC_uvlo}				2.85		V
$V_{CC\_uvlo\_hys}$				75		mV
IV_{CC}	VCC Sourcing current limit		20	70		mA
$V_{UVLOSEN}$	Under voltage Lockout reference voltage	V_{UVLO} ramping up	1.34	1.42	1.5	V
I_{UVLO}	UVLO source current		3	4.75	6.5	uA
V_{UVLOSD}	UVLO shut down voltage	V_{UVLO} ramping down	0.55	0.65	0.75	V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		1.256	1.275	1.294	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	190	390	590	uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	340	560	710	uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	-150	-95	-40	uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V	1.9	2.55	3.2	V
V_{COMP_L}	COMP low clamp	V_{FB}=1.7V	0.4	0.88	1.2	V
Gate Driver						
R_{DSON_TOP}	Driver switch on resistance(top)	I_{DR}=0.1A		3		
R_{DSON_LOW}	Driver switch on resistance(bottom)	I_{DR}=0.1A		2		
Current Sense						
Vsense	Current sense threshold		120	146	170	mV
V_{SL}(2)	Internal compensation Ramp voltage			90		mV

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft start						
T_{SS}	Soft-start Time			14		ms
Switching Frequency						
F_{SW}	Switching frequency	R				

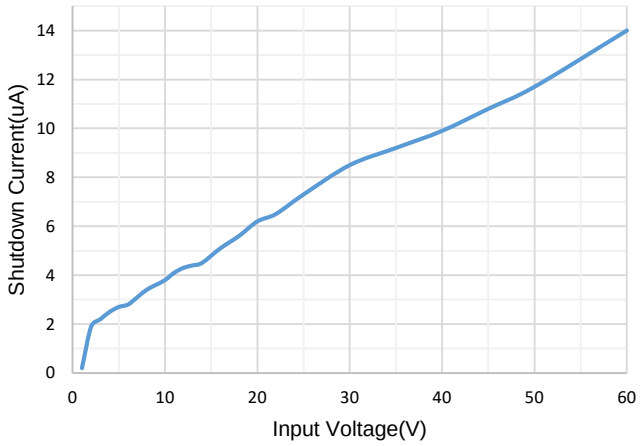


Figure 1. ISD vs. Input Voltage

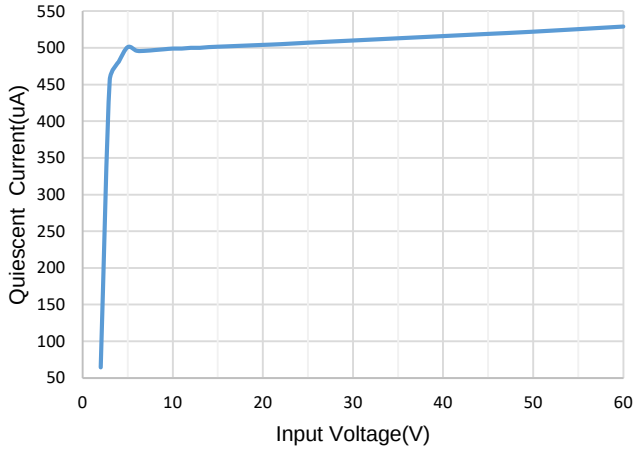


Figure 2. IQ vs. Input Voltage

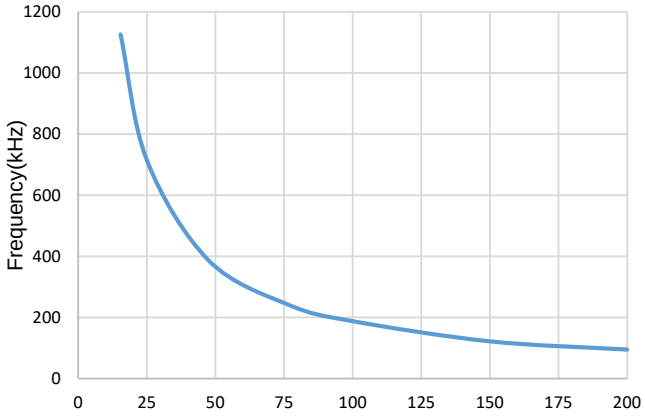


Figure 3. Switching Frequency vs. RT

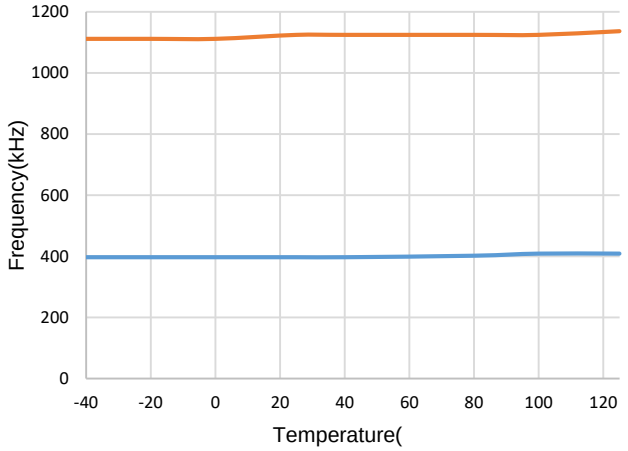


Figure 4. Switching Frequency vs. Temperature

Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

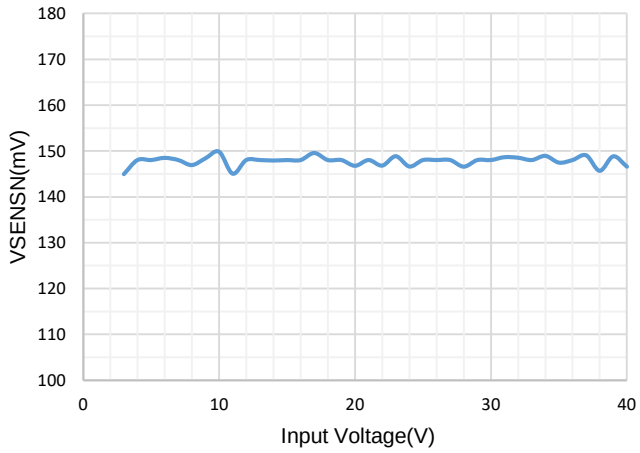


Figure 7. VSENSN vs. Input Voltage

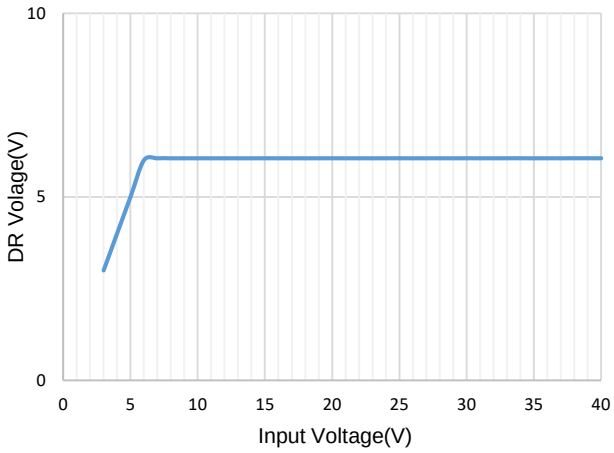


Figure 8. DR Volage vs. Input Voltage

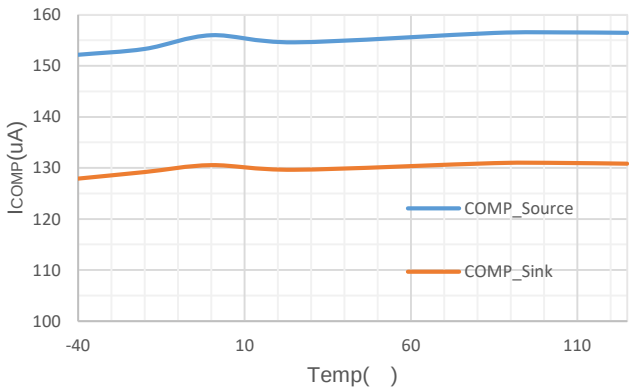


Figure 9. COMP Current vs. Temperature

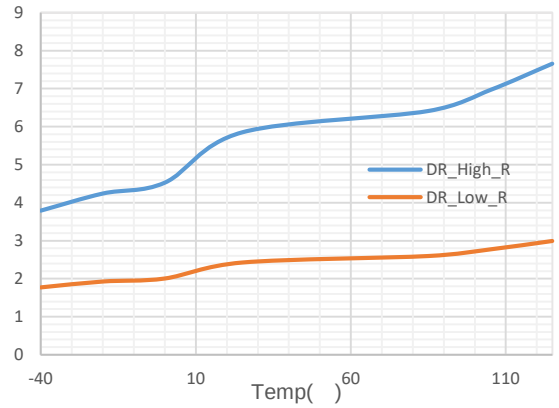


Figure 10. DR Resistance vs. Temperature

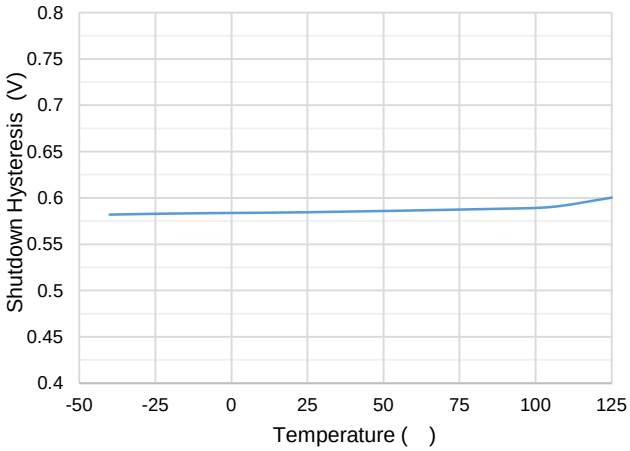
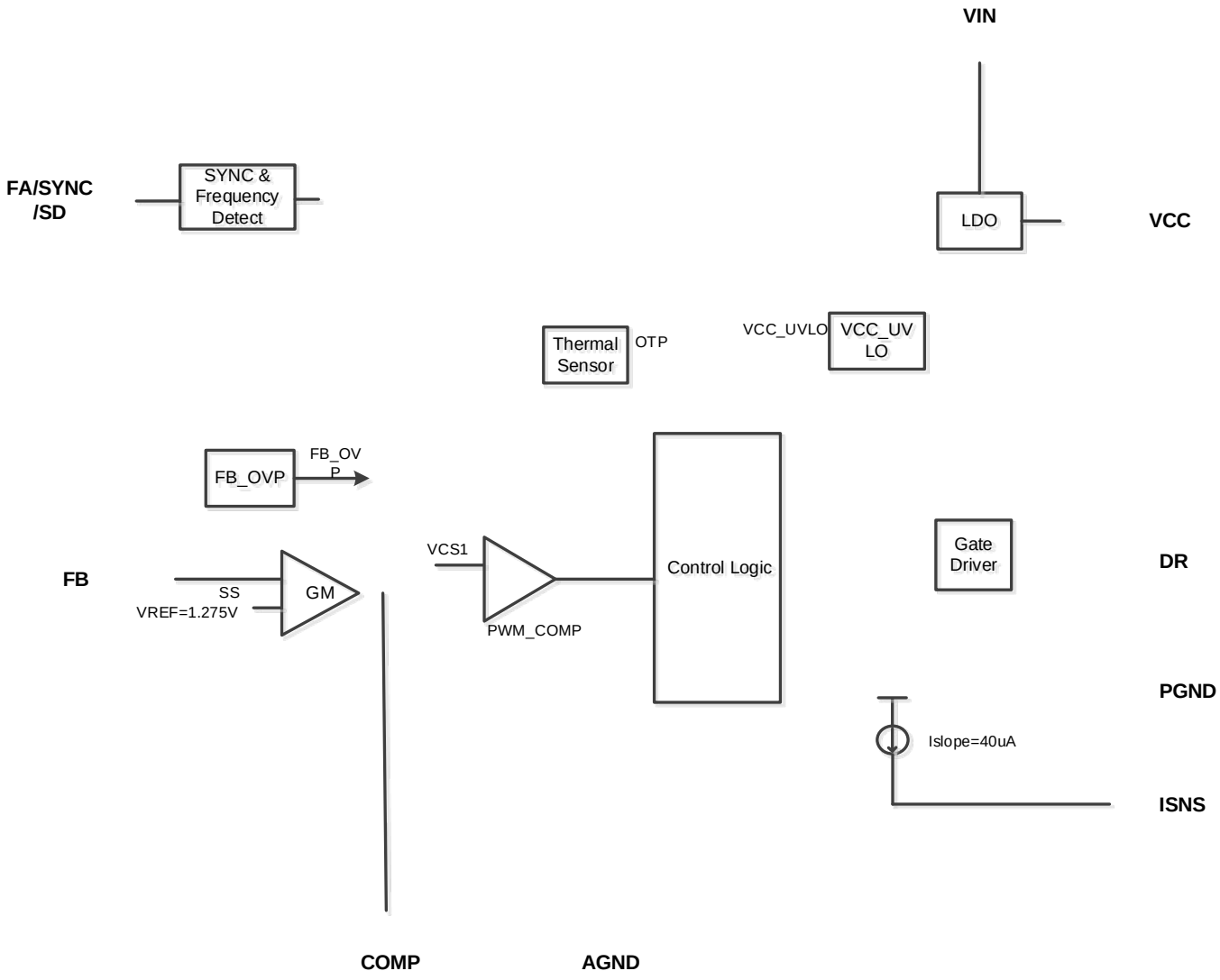


Figure 11. Shutdown Threshold Hysteresis vs. Temperature



Overview

The SCT81624 device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISNS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81624 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81624 works at Pulse skip mode to further increase the efficiency in light load condition.

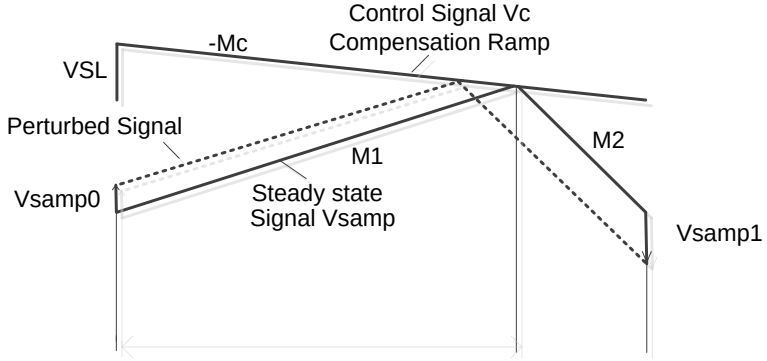
The quiescent current of SCT81624 is 415uA typical under no-load condition and no switching. Disabling the device, the typical supply shutdown current on VIN pin is 3.9

Overvoltage Protection

The SCT81624 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.36V (typ.), OVP is triggered. OVP will cause the DR pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81624 begins switching again when the feedback voltage reaches 1.29V (typ.).

Slope Compensation Ramp

The SCT81624 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycle is greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.



A typical value for factor K is 40 µA.

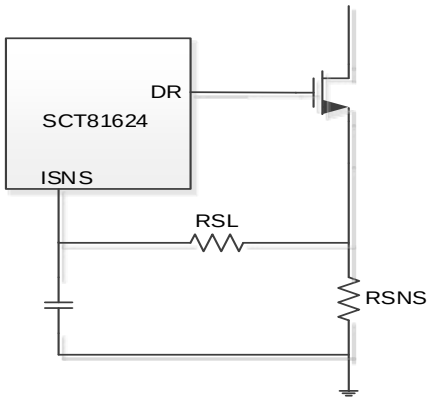


Figure14. External RSL to increase slope compensation

-96 1.5o(k3-7.5lt)-4-27 a(k 5.2)(gmk3-7.5emk3-32. (ab9)-2.T(022 Tc 010 16.4 u18Tj 316 16)Tj E[3yp(k)-33 .(st)-12. (022

Enable and Under Voltage Lockout Threshold

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.42 V typical) when the input voltage is in the desired operating range. The values of R1 and R2 can be calculated as shown in Equation 14 and Equation 15.

$$R1 = \frac{V_{IN(ON)} - V_{IN(OFF)}}{I_{UVLO}} \quad (14)$$

where

$V_{IN(ON)}$ is the desired start-up voltage of the converter
$V_{IN(OFF)}$ is the desired turnoff voltage of the converter.

$$R2 = R1 * \frac{V_{UVLOEN}}{V_{IN(ON)} - V_{UVLOEN}} \quad (15)$$

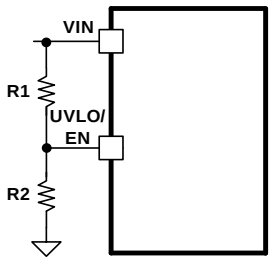
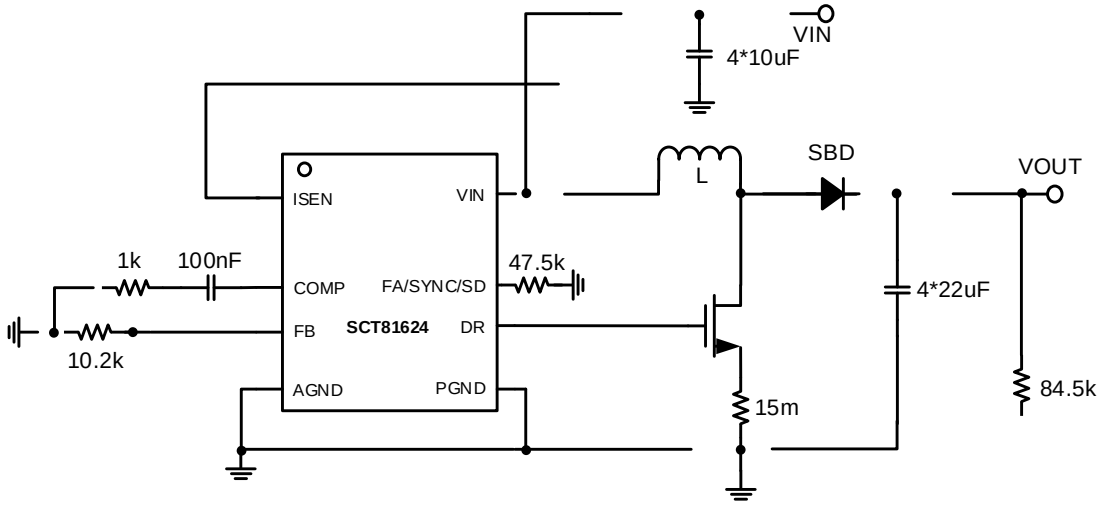


Figure19. System UVLO Resistor Divider

Typical Application (Boost)



Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as in Equation 16

$$= \frac{\times}{\times} \quad (16)$$

Where

V_{OUT} is the output voltage of the boost converter
I_{OUT} is the output current of the boost converter
V_{IN} is the input voltage of the boost converter

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in Equation 17.

$$= \frac{1}{\times \left(\frac{}{} + \frac{}{}\right) \times} \quad (17)$$

Where

I_{LPP} is the inductor peak-to-peak current
L is the inductance of inductor
f_{SW} is the switching frequency
V_{OUT} is the output voltage
V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in Equation 18

$$= \quad + \frac{}{2} \quad (18)$$

Set the current limit of the SCT81624 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 19.

$$I_{CIN(RMS)} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times fsw} \quad (19)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10 µF to 40 µF. If a value lower than 10 µF is used, then problems with impedance interactions or switching noise can affect the SCT81624. To improve performance, especially with Vin below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly. A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3 4x 22 ceramic output capacitors work for most applications.
placed as close as possible to the switch node Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 20 and 21 to calculate the minimum required effective capacitance, C_{OUT}.

$$= \frac{(\quad - \quad) \times}{\times \quad \times} \tag{20}$$

$$= \quad \times \tag{21}$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a Boost is given by

$$V_{SW\_PEAK} = V_{IN} + V_D \tag{22}$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{LPEAK} \tag{23}$$

The RMS current through the MOSFET is calculated by:

$$I_{Q\_RMS} = \sqrt{(I_{LDC}{}^2 + \frac{I_{LPP}}{12}) * D} \tag{24}$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + \left(V_O + V_{IN\_MIN}\right) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \tag{25}$$

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using Equation 26.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (26)$$

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

Figure 21. Power up(Iload=2A)

Figure 22. Power down(Iload=2A)

Figure 23. Over current protection (Iload=5A)

Figure 24. Over current recovery (Iload=5A)

Typical Application(Sepic)

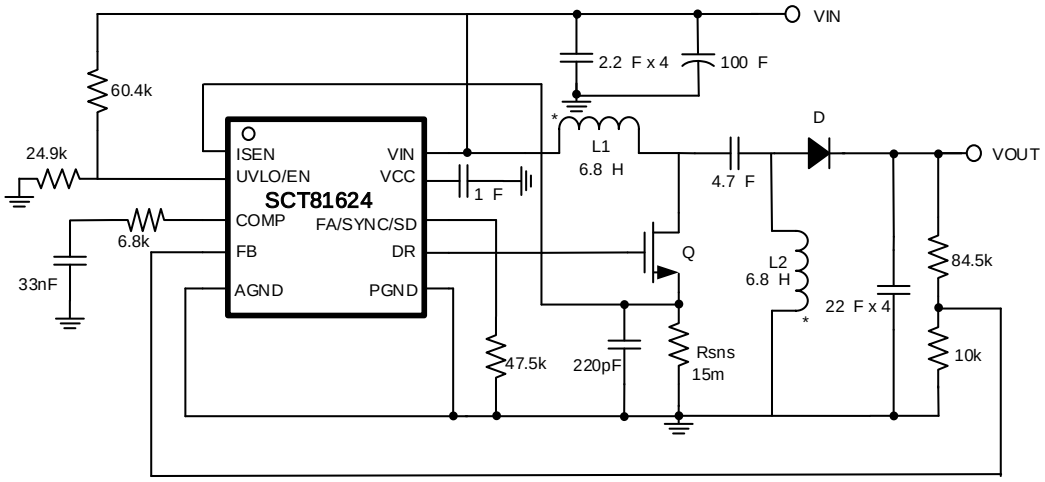


Figure 27. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN\_MIN}} \times 40\% \quad (27)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (28)$$

Normally we can select equal value for the inductors L1 and L2, derived as:

$$L_1 = L_2 = L = \frac{V_{IN\_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (29)$$

Where

f_{SW} is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$I_{L1\_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN\_MIN}} \times (1 + \frac{40\%}{2}) \quad (30)$$

$$I_{L2\_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \quad (31)$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN\_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (32)$$

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a SEPIC is given by:

$$V_{SW\_PEAK} = V_{IN} + V_O + V_D \quad (33)$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{L1\_PEAK} + I_{L2\_PEAK} \quad (34)$$

The RMS current through the MOSFET I s calculated by:

$$I_{Q\_RMS} = I_O \times \sqrt{\frac{(V_O + V_{IN\_MIN} + V_D) \times (V_O + V_D)}{V_{IN\_MIN}^2}} \quad (35)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + (V_O + V_{IN\_MIN}) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (36)$$

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} = V_{IN\_MAX} + V_{O\_MAX} \quad (37)$$

The diode should also be capable to flow switch peak current I_{Q_PEAK}.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (38)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS\_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN\_MIN}}} \quad (39)$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN\_RMS} = \frac{\Delta I_{L1}}{\sqrt{12}} \quad (40)$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100 F in total or higher value is strongly recommended in order to provide stable input supply.

Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$\Delta V_{OUT} = \frac{I_O \times D_{MAX}}{C_{OUT} \times f_{SW}} + ESR \times \left(I_{L1\_PEAK} + I_{L2\_PEAK} \right) \quad (41)$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$C_{OUT} \geq \frac{I_O \times D_{MAX}}{\Delta V_{OUT} \times f_{SW}} \quad (42)$$

The output capacitor must have an enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (43)$$

Application Waveforms
Vin=5V, Vout=12V, unless otherwise noted

Figure 29. Power up(Iload=2A)

Figure 30. Power down(Iload=2A)

Figure 31.

Layout Guideline

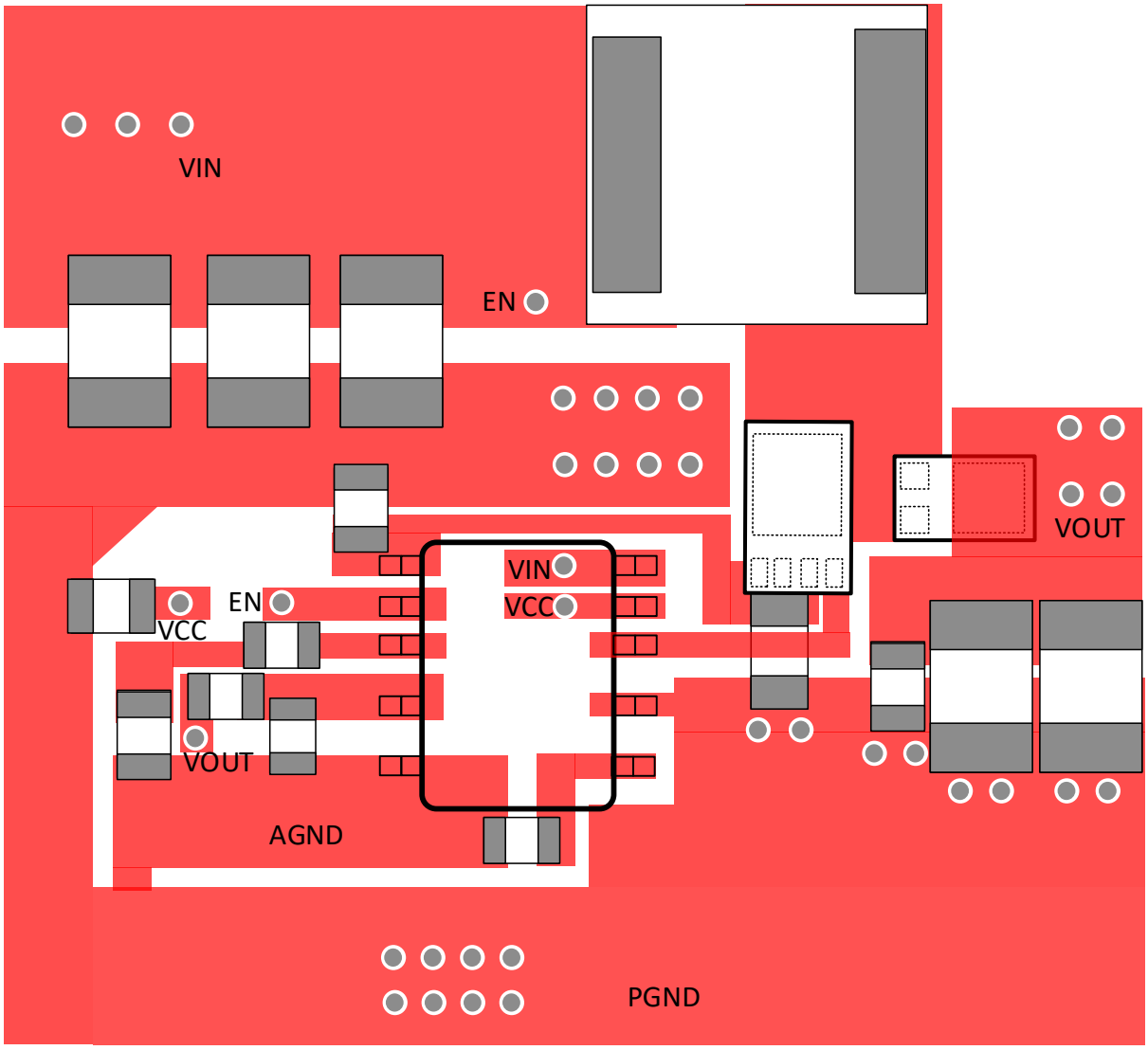
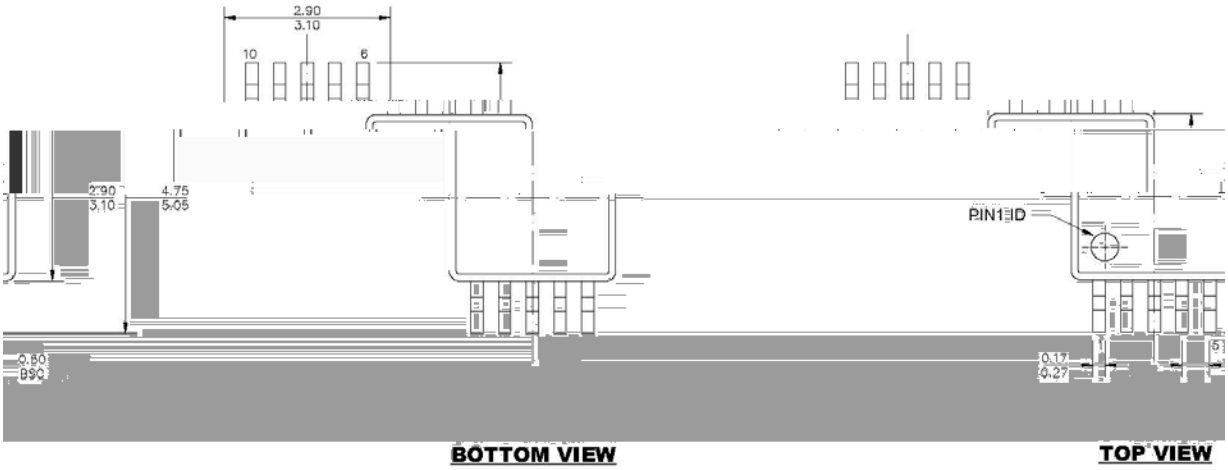
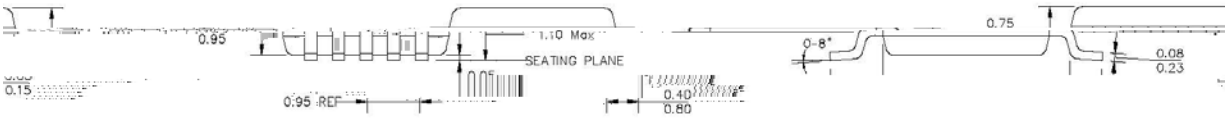


Figure 35. BOOST PCB Layout



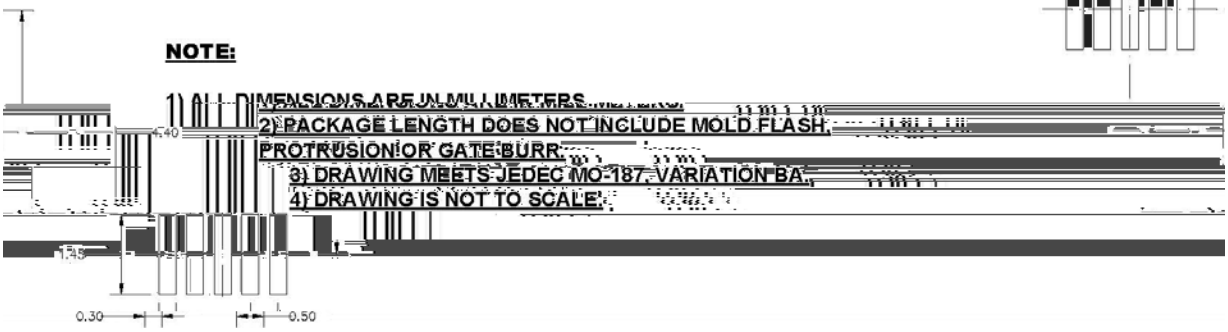
BOTTOM VIEW TOP VIEW



SIDE VIEW FRONT VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) DRAWING MEETS JEDEC MO-187, VARIATION BA.
4) DRAWING IS NOT TO SCALE.



RECOMMENDED LAND PATTERN

