

Revision 1.0: Production
Revision 1.1: Update Shutdown current in EC table

SCT9431QFSA	9431Q	FCQFN2X3-9L

1) For Tape & Reel, Add Suffix R (e.g. SCT9431QFSAR)

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT

BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
NC	7	NC
GND	8	Power ground. Must be soldered directly to ground plane.
SW	9	Switching node of the buck converter.

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	3.8	36	V
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	Operating junction temperature	-40	150	°C

V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-1	+1	kV

$R_{\theta JA}$	Junction to ambient thermal resistance(1)	61.33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.24	
Ψ_{JB}	Junction-to-board characterization parameter(1)	5.43	
$R_{\theta JCtop}$	Junction to case(top) thermal resistance(1)	62.99	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	5.6	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT9431Q is mounted. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT9431Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

V_{IN}=12V, T_J=-40°C~150°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		3.8		36	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	3.3	3.5	3.7	V
	Hysteresis			420		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		0.6	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		22	40	uA
V_{EN_H}	Enable high threshold		1.08	1.18	1.28	V
V_{EN_L}	Enable low threshold		0.98	1.1	1.18	V
I_{EN_L}	Enable pin input current	EN=1V	1	1.5	2	uA
I_{EN_H}	Enable pin input current	EN=1.5V		4		uA
R_{DSON_H}	High side FET on-resistance			74	130	mΩ
R_{DSON_L}	Low side FET on-resistance			40	70	mΩ
V_{FB}	Feedback Voltage	T_J =25℃	0.792	0.8	0.808	V
		T_J =-40℃-150℃	0.788	0.8	0.812	V
I_{LIM_HSD}	HSD peak current limit	T_J =25℃	4.0	4.5	5.0	A
		T_J =-40℃-150℃	3.7	4.5	5.3	A
I_{LIM_LSD}	LSD valley current limit			4		A
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V, T_J =25℃	350	400	450	kHz
		V_{IN}=12V, V_{OUT}=5V, T_J =-40℃-150℃	330		470	
t_{ON_MIN}	Minimum on-time			100		ns
t_{SS}	Internal soft-start time			4		ms
V_{OVP}	Output OVP threshold	V_{OUT} rising Hysteresis		110 5		% %
T_{SD}	Thermal shutdown threshold*	T_J rising Hysteresis		170 25		°C

*Derived from bench characterization

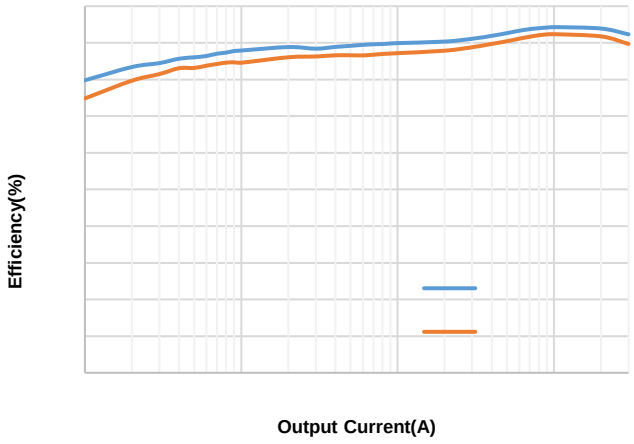


Figure 1. Efficiency vs Load Current

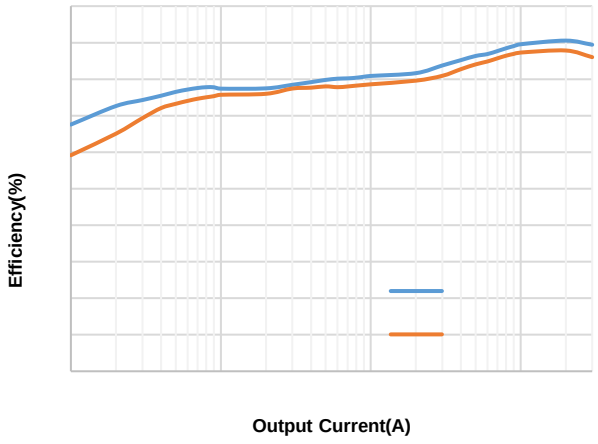


Figure 2. Efficiency vs Load Current

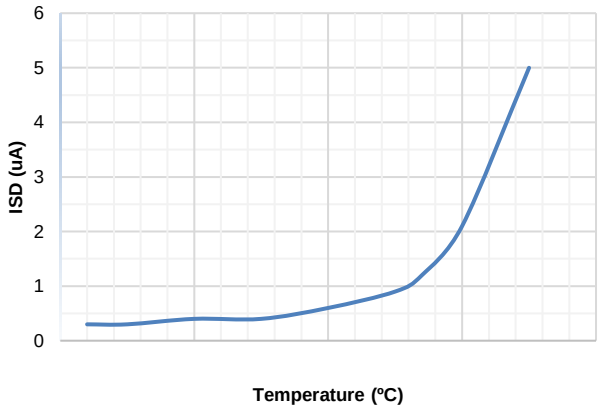


Figure 3. Shut-down Current vs Temperature

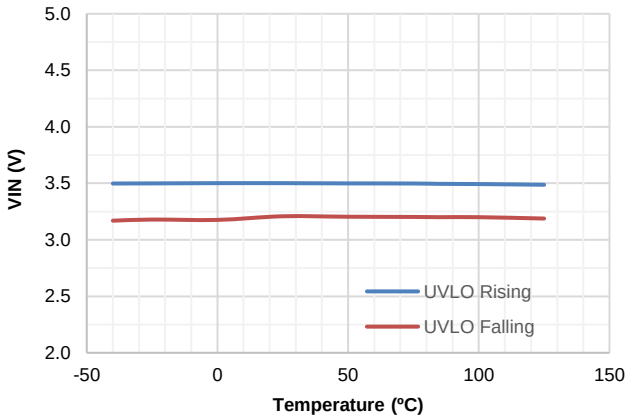


Figure 4. VIN UVLO vs Temperature

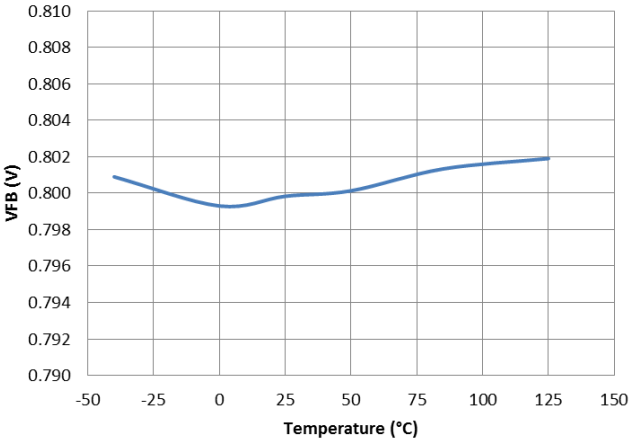


Figure 5. Reference Voltage vs Temperature

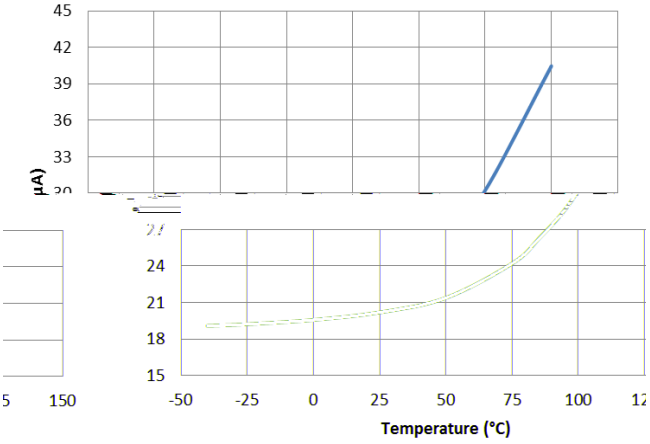
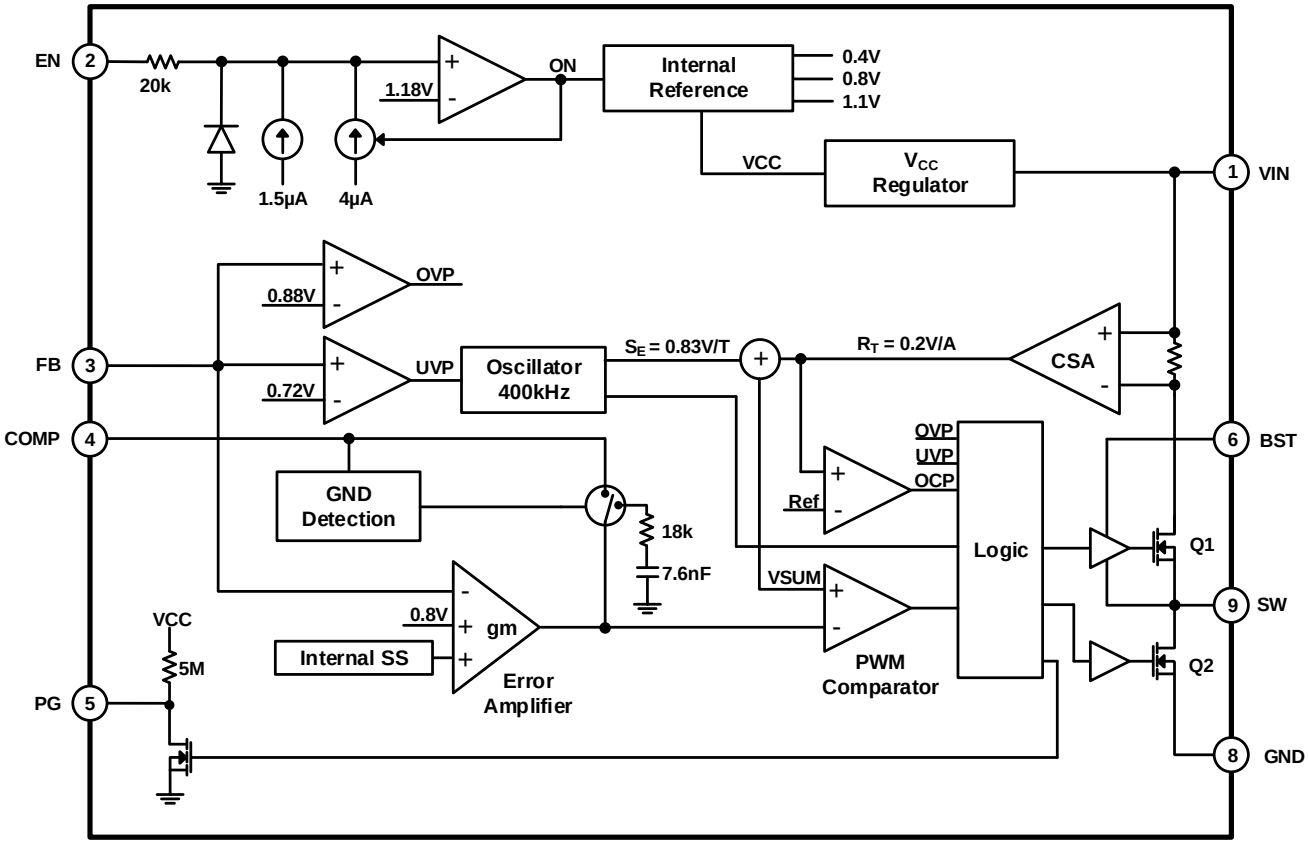


Figure 6. I_Q vs. Temperature, IOUT = 0A


EN
2
20k
1.18V
ON
Internal Reference
0.4V
0.8V
1.1V
VCC
VCC Regulator
1
VIN
1.5µA
4µA
0.88V
OVP
FB
3
0.72V
UVP
Oscillator 400kHz
SE = 0.83V/T
RT = 0.2V/A
CSA
COMP
4
GND Detection
18k
7.6nF
Ref
OVP
UVP
OCP
Logic
6
BST
Q1
VSUM
0.8V
gm
Internal SS
Error Amplifier
PWM Comparator
9
SW
Q2
VCC
5M
PG
5
8
GND

The SCT9431Q device is 3.8V-36V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 400kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current via the CSA block, rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The internal loop compensation network and the built-in 4ms soft-start simplify the SCT9431Q footprints, and minimize the off-chip component counts. The quiescent current of SCT9431Q is 22uA typical under no-load condition and no switching. When disabling the device, the shutdown current of SCT9431Q is only 1μA. The SCT9431Q works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT9431Q device implements Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%. FSS reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. The converter further dampens high frequency radiated EMI noise through the use of its proprietary gate driver scheme to achieve a ringing-free switching node voltage without sacrificing the MOSFET switching times.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9431Q device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

In heavy load condition, the SCT9431Q forces the device operating at PWM

$ M ^ ľ .

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9431Q enables all functions and the device starts soft-start phase. The SCT9431Q has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (tm ing a voltage h] 0 id.

delayed by 220μs to prevent false triggering.

The SCT9431Q have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Both SCT9431Q feature output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage, the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

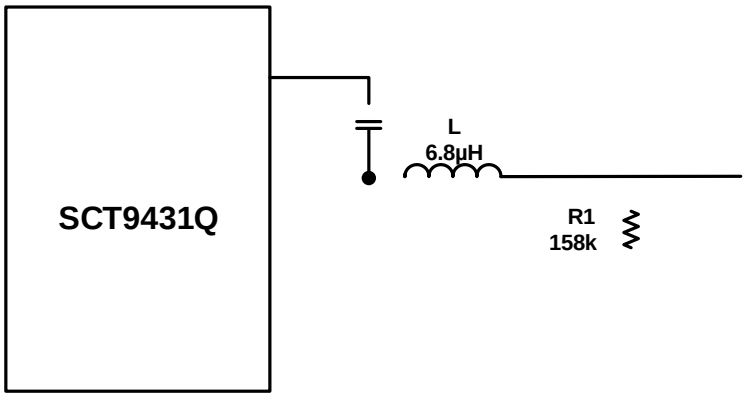
The high-side MOSFET Q1 has minimum on-time 100ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9431Q intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9431Q implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

Once the junction temperature in the SCT9431Q exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 145°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.



Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.03V
Switching Frequency	400kHz

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT9431Q. cn urrel m š ue f l ¡ l ¡

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

C_{IN} is the input capacitor value
f_{sw} is the converter switching frequency
I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make sure the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully.

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1 2x 22µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

(6)

Where

$V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
ΔI_{LPP} is the inductor peak to peak ripple current, equal to $k_{IND} * I_{OUT}$.
f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

(7)

The output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 40 kHz (—) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

(8)

Where

G_M is the transfer conductance of the error amplifier (300uS).
G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

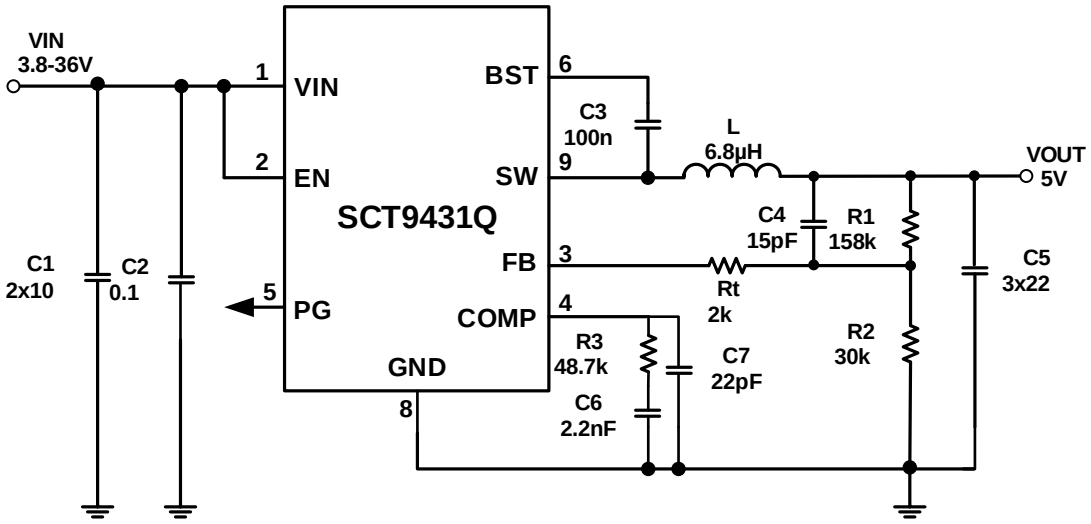
The SCT9431Q has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

(10)

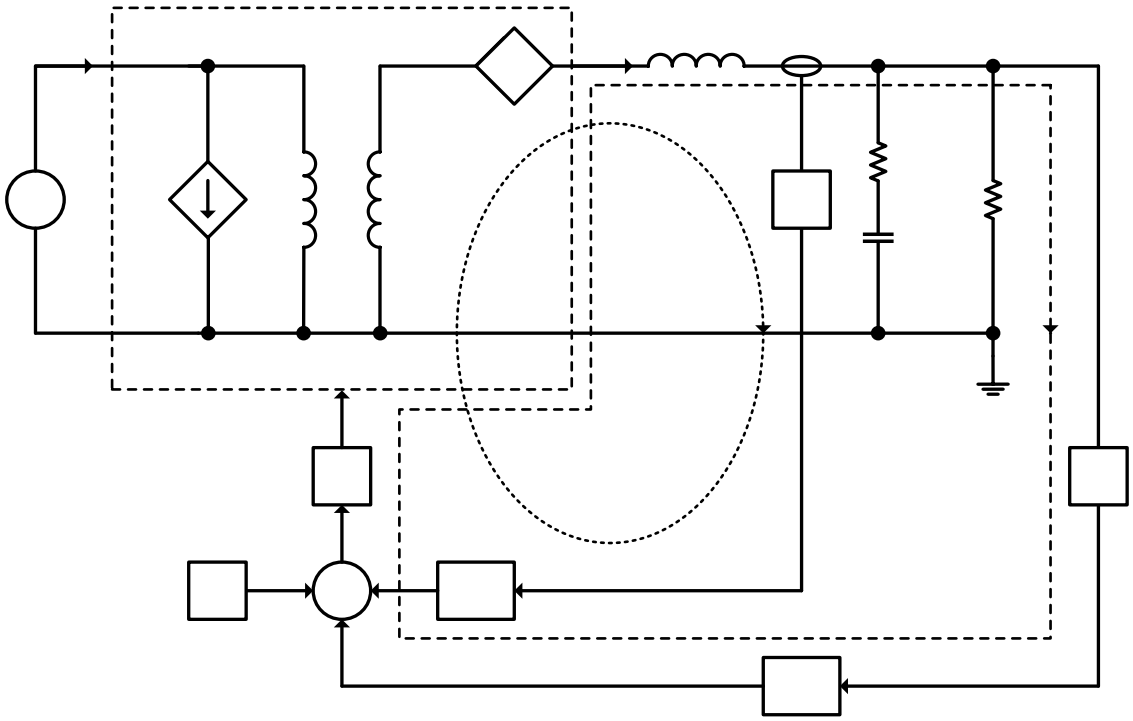
The SCT9431Q features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 9. Use equation (11) to calculate the resistor divider values.

(11)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.
Table 1 is the recommend external components for the application with integrated loop compensation for SCT9431Q.

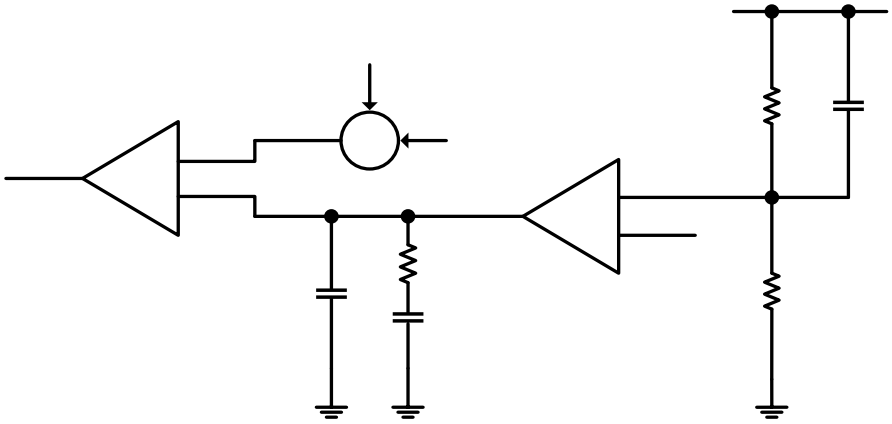


When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses constant frequency peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. The system becomes a single order system. It is much easier to design a type II compensator (Figure 12) to stabilize the loop than in case of a voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 11 shows the small signal model of the synchronous buck regulator.



Where:

$T_v(S)$ is the voltage loop
$T_i(S)$ is the current loop
K(S) is the voltage sense gain
$-A_v(S)$ is the feedback compensation gain
$H_e(S)$ is the current sampling function
F_m is the PWM comparator gain
V_{in} is the DC input voltage
D is the duty cycle
R_c is the ESR of the output capacitor, COUT
R_o is the output load resistance$\hat{v}_{in}$ is the AC small-signal input voltage
$\hat{i}_{in}$ is the AC small-signal input current
$\hat{d}$ is the modulation of the duty cycle
$\hat{i}_L$ is the AC small signal of the inductor current
$\hat{v}_o$ is the AC small signal of output voltage
$\hat{v}_{comp}$ is the AC small signal voltage of the compensation network



Transfer function of Figure 12 is expressed in the following equation,

(12)

Where:

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_k 5 ŋ

Vin=12V, Vout=5V, unless otherwise noted

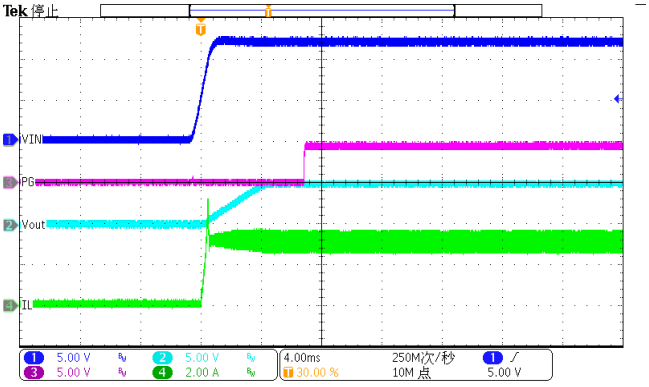


Figure 13. Power up(Iload=3A)

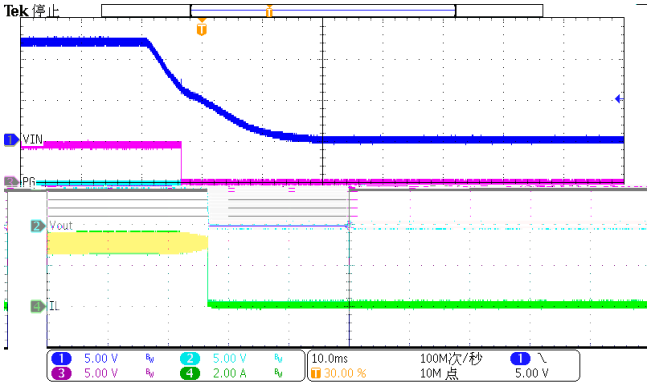


Figure 14. Power down(Iload=3A)

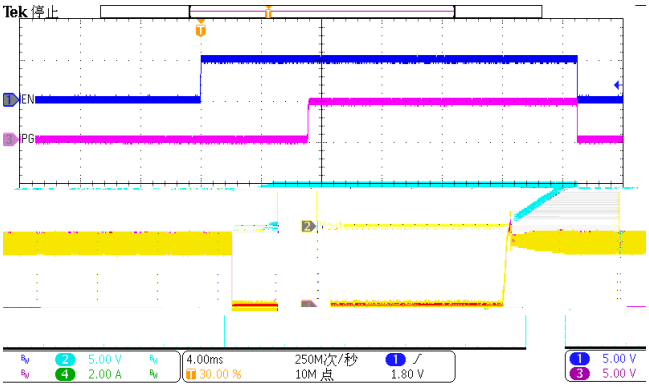


Figure 15.Enable (Iload=3A)

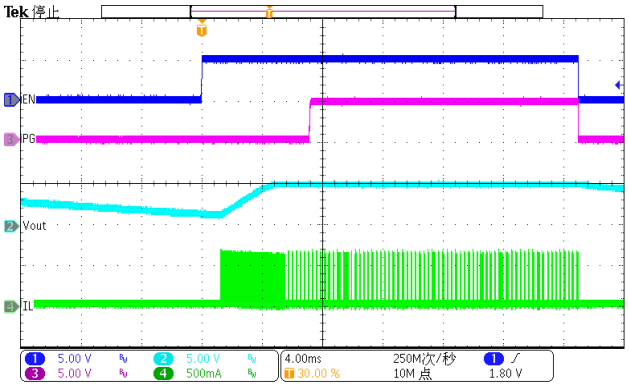


Figure 16. Enable (Iload=10mA)

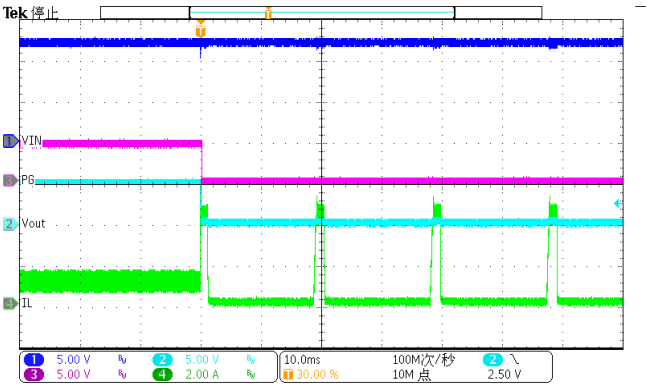


Figure17. Normal to Hard Short

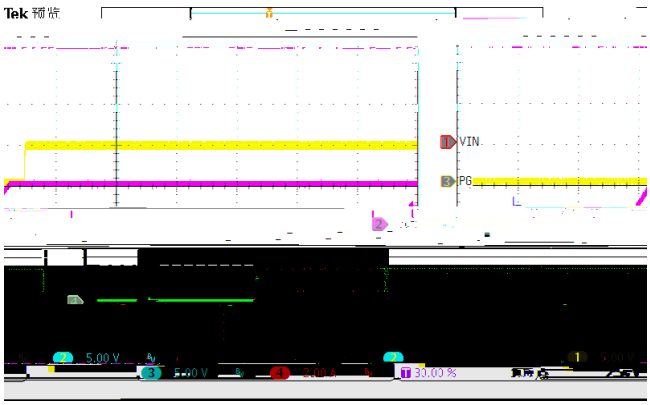


Figure 18. Hard Short Recovery

Vin=12V, Vout=5V, unless otherwise noted

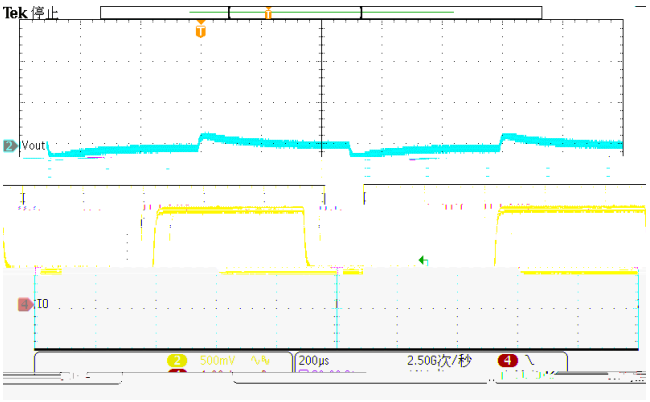


Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

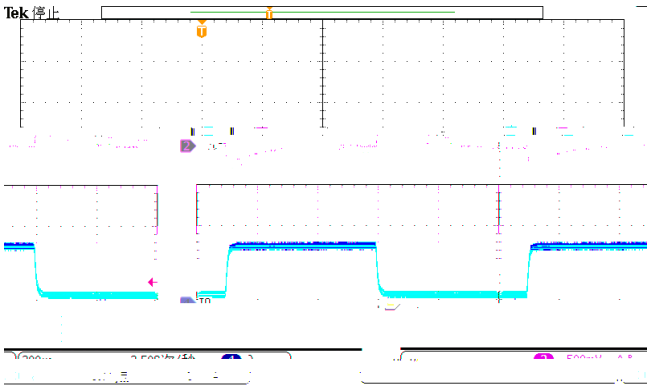


Figure 20. Load Transient (0.3A-2.7A, 1.6A/us)

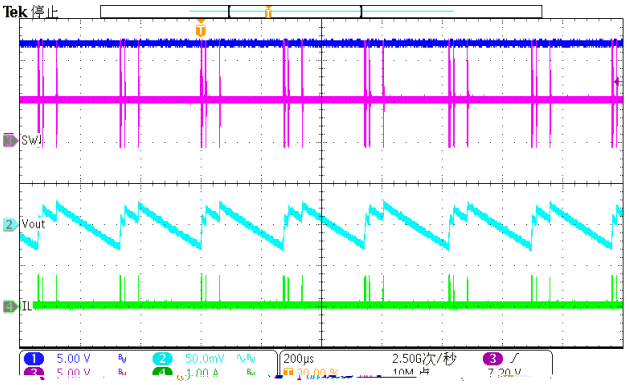


Figure 21. Output Ripple (Iload=10mA)

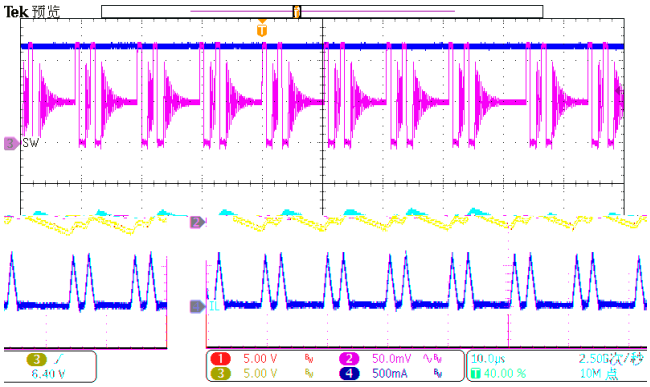


Figure 22. Output Ripple (Iload=0.1A)

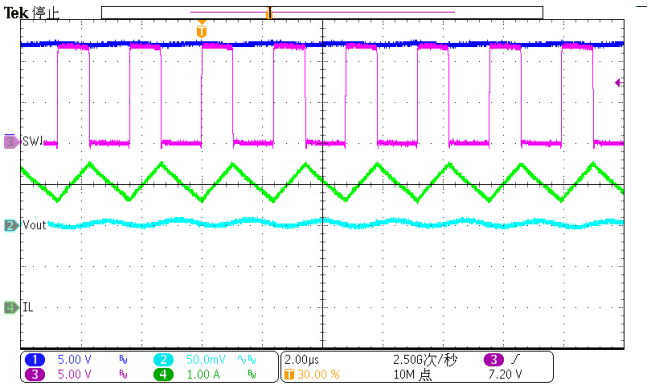


Figure 23. Output Ripple (Iload=3A)

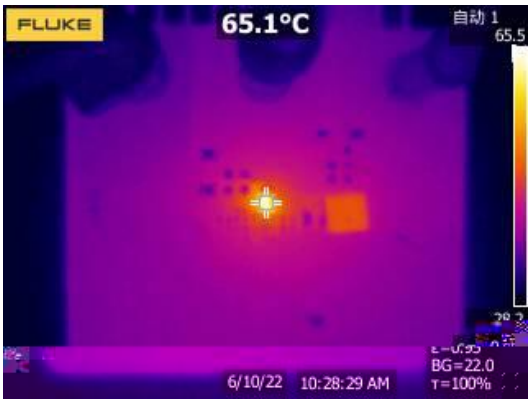
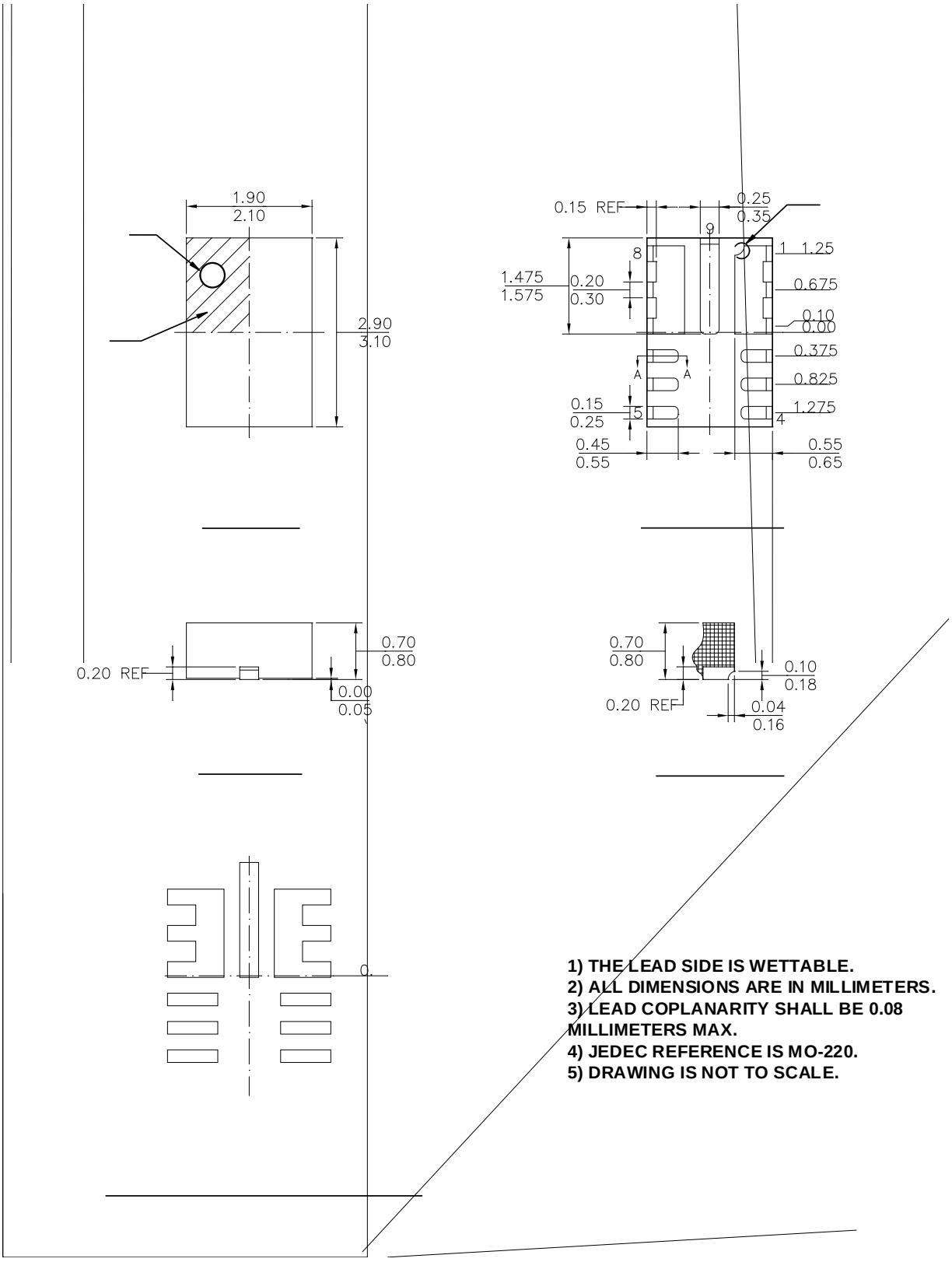


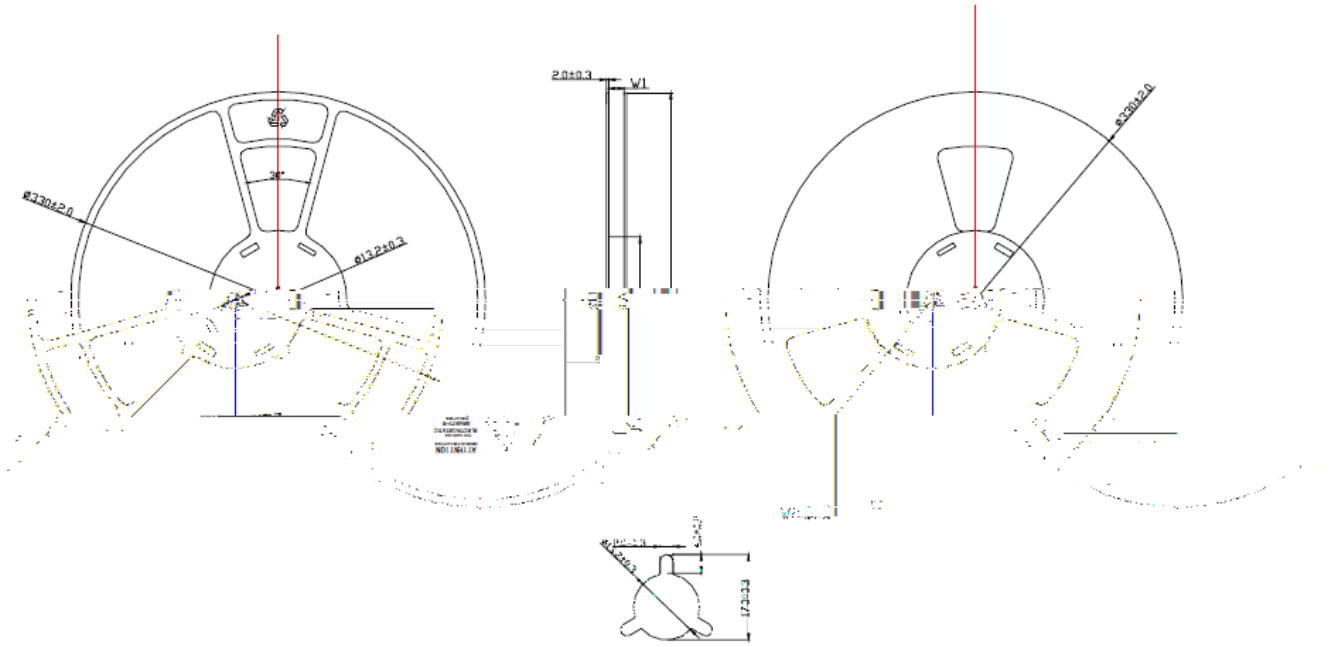
Figure 24. Thermal, 12VIN, 5Vout, 3A

Figure 25 and Figure 26 are the recommended PCB layout of SCT9431Q with or without external compensation network.

1. The SCT9431Q works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias under both the thermally exposed GND pad and GND plane for heat dissipation to all the GND layers.
8. Add as many vias under both the thermally exposed VIN pad and VIN plane for heat dissipation to all the VIN layers.



Orderable Device	Package Type	Pins	SPQ
SCT9431QFSAR	QFN 2mmx3mm	9	5000



	328	330	332
	99	100	101
	12.4	-	-
	-	-	19.4