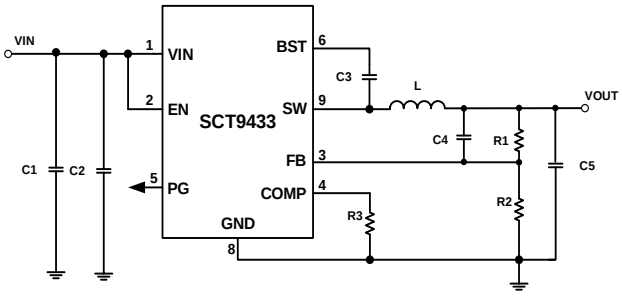
- 3.8V-36V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- EMI Reduction
  - Proprietary Gate Design for Switching Node Ringing-free
  - Frequency Spread Spectrum (FSS)
- Pulse Skipping Mode (PSM) with 22uA Quiescent Current in Light Load Condition
  - Up to 81% Efficiency at 1mA Light Load
  - Up to 87% Efficiency at 10mA Light Load
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 74mΩ R_{dson} High Side MOSFET and 40mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 800kHz Switching Frequency
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Output Over Voltage Protection
- Thermal Shutdown Protection at 170°C

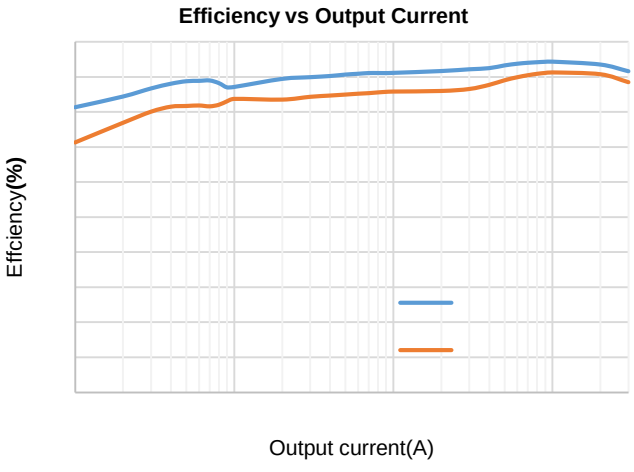
The SCT9433 are 3A synchronous buck converters with up to 36V wide input voltage range, which fully integrates an 74mΩ high-side MOSFET and a 40mΩ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9433 adopts peak current mode control with integrated compensation network. The SCT9433 supports the Pulse Skipping Modulation (PSM) with typical 22uA Ultra-Low Quiescent.

The SCT9433 are optimized for Electromagnetic Interference (EMI) reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. The converter features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The SCT9433 offer output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile QFN-9L 3mm X 2mm package.

- Automotive System
- Industrial Control System
- General Consumer





Revision 1.0: Production

!	!	%
SCT9433FSA	9433	FCQFN2X3-9L

1) For Tape & Reel, Add Suffix R (e.g. SCT9433FSAR)

Over operating free-air t0 54mpratira frrr ggopieraTI-2(r)s6(g)e( )-3(f)n(r

NC	7	NC
GND	8	Power ground. Must be soldered directly to ground plane.
SW	9	Switching node of the buck converter.

Over operating free-air temperature range unless otherwise noted

!	%	!	!	
V_{IN}	Input voltage range	3.8	36	V
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	Operating junction temperature	-40	150	°C

!	%	!	!	
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV

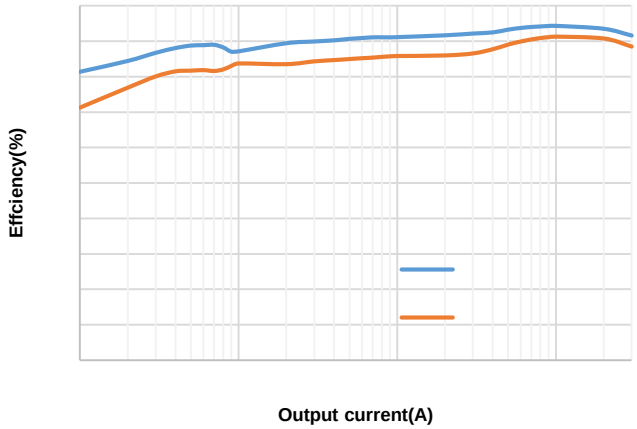


Figure 1. Efficiency vs Load Current

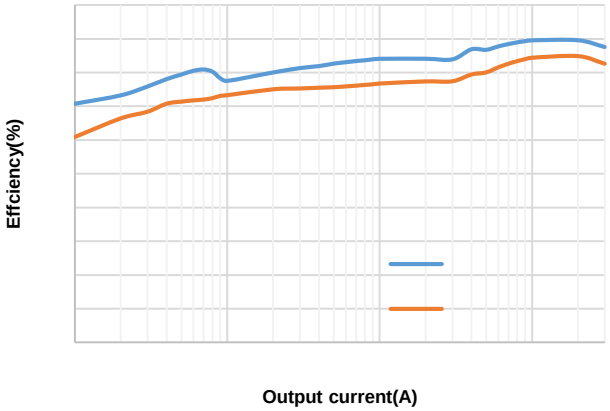


Figure 2. Efficiency vs Load Current

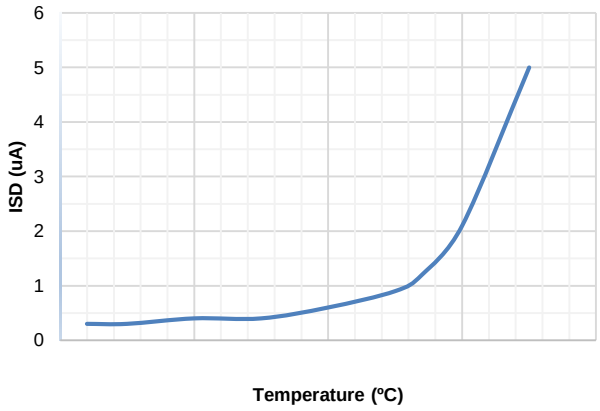


Figure 3. Shut-down Current vs Temperature

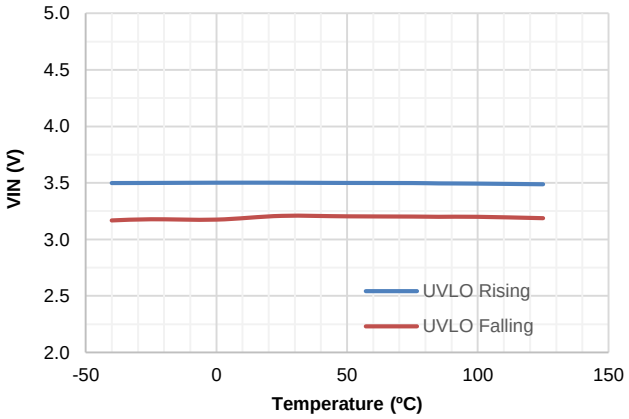


Figure 4. VIN UVLO vs Temperature

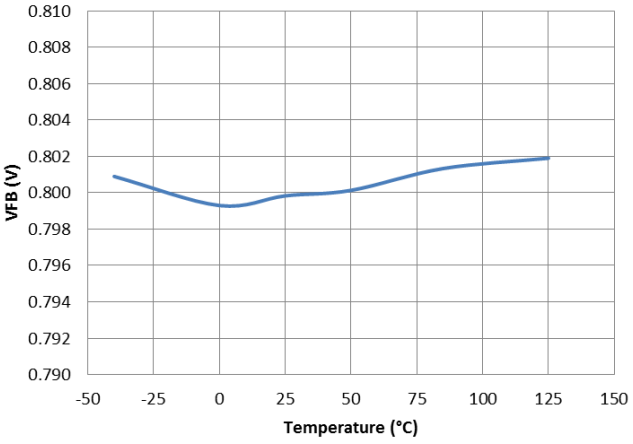


Figure 5. Reference Voltage vs Temperature

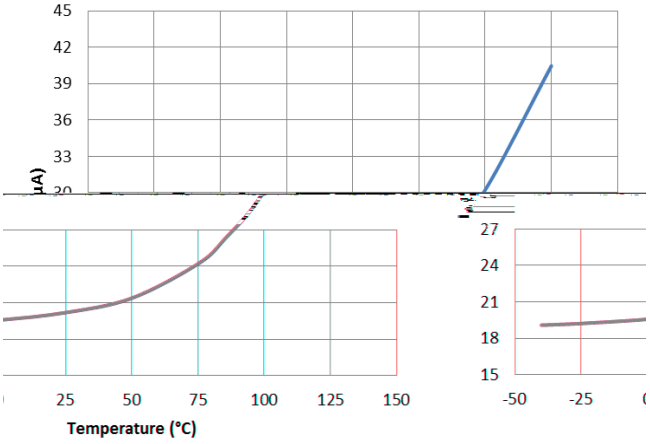
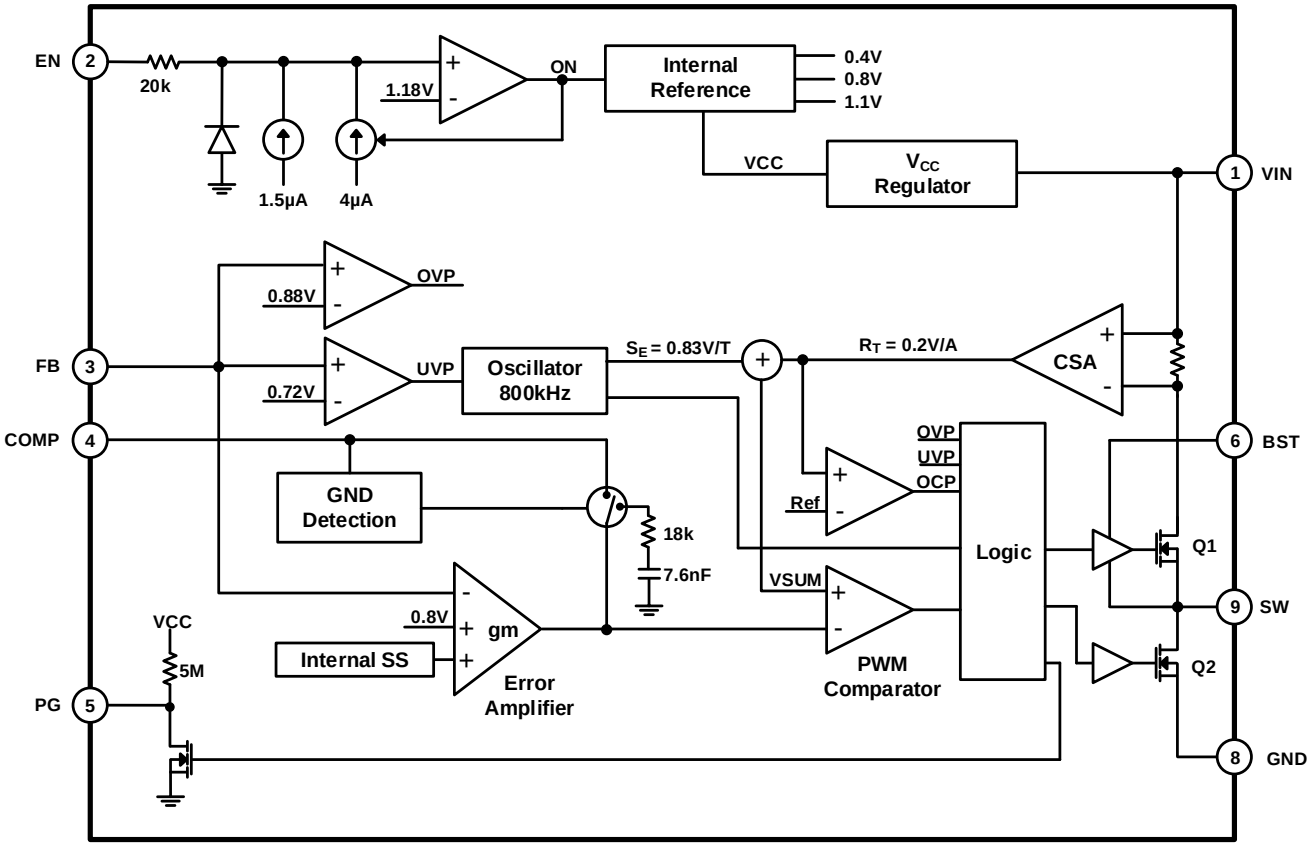


Figure 6. I_Q vs. Temperature, IOUT = 0A


EN
2
20k
1.18V
ON
Internal Reference
0.4V
0.8V
1.1V
VCC
VCC Regulator
1
VIN
1.5μA
4μA
OVP
0.88V
FB
3
UVP
0.72V
Oscillator 800kHz
SE = 0.83V/T
RT = 0.2V/A
CSA
COMP
4
GND Detection
18k
7.6nF
Ref
OVP
UVP
OCP
Logic
6
BST
Q1
VSUM
9
SW
Q2
VCC
5M
0.8V
gm
Internal SS
Error Amplifier
PWM Comparator
PG
5
8
GND

-

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The SCT9433 device is 3.8V-36V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 800kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current via the CSA block, rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The internal loop compensation network and the built-in 4ms soft-start simplify the SCT9433 footprints, and minimize the off-chip component counts. The quiescent current of SCT9433 is 22uA typical under no-load condition and no switching. When disabling the device, the shutdown current of SCT9433 is only 1μA. The SCT9433 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 89% at 5mA load condition.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT9433 device implements Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%. FSS reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. The converter further dampens high frequency radiated EMI noise through the use of its proprietary gate driver scheme to achieve a ringing-free switching node voltage without sacrificing the MOSFET switching times.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9433 device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

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In heavy load condition, the SCT9433 forces the device operating at PWM mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9433 enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

The SCT9433 is designed to operate from an input voltage supply range between 3.8V to 36V. At least a 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

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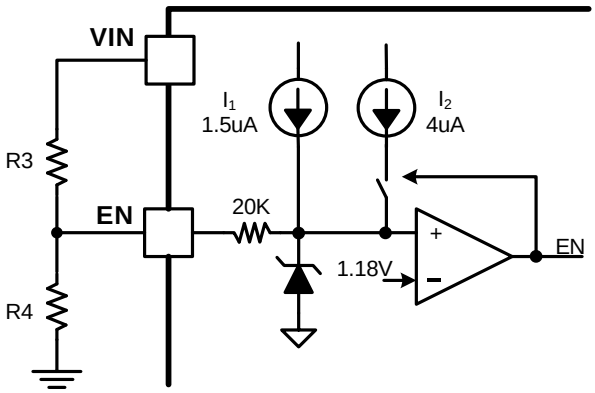
The SCT9433 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9433 enables all functions and the device starts soft-start phase. The SCT9433 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.



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(1)

(2)

Where:

- V_{start}: Vin rise threshold to enable the device
- V_{stop}: Vin fall threshold to disable the device
- I_1=1.5uA
- I_2=4uA
- V_{ENR}=1.18V
- V_{EMF}=1.1V

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The SCT9433 has an open-drain output that is actively held low during soft start period until the output voltage reaches 90% of the target output. When the output voltage is outside of its regulation by -10%, the PG will pull low until the output returns to set value. The PG low to high transition is delayed by 2.5ms while the falling edge PG is

delayed by 220μs to prevent false triggering.

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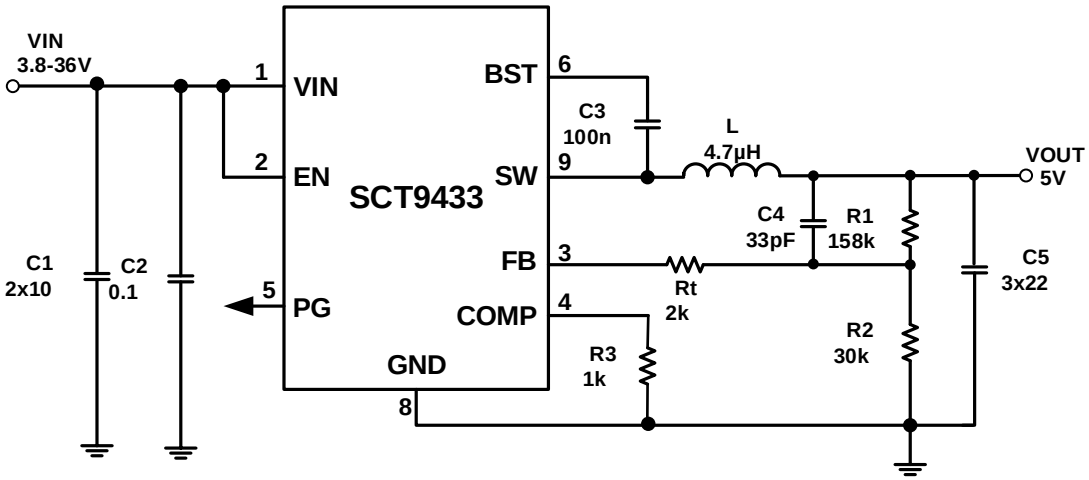
The SCT9433 have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1



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Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.03V
Switching Frequency	800kHz

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT9433.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

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For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1 2x 22µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitan

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The SCT9433 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

(10)

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The SCT9433 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 9. Use equation (11) to calculate the resistor divider values.

(11)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.
Table 1 is the recommend external components for the application with integrated loop compensation for SCT9433.

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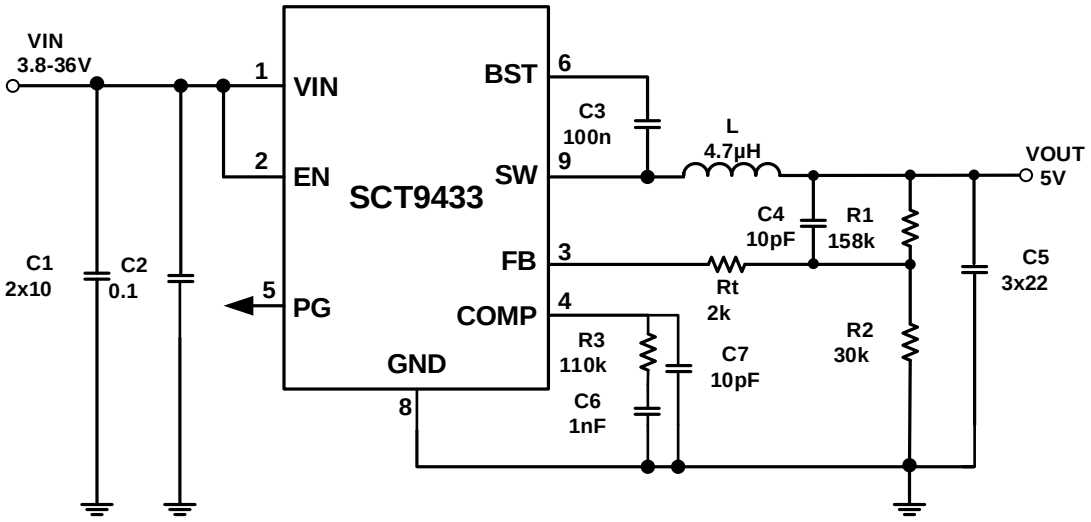

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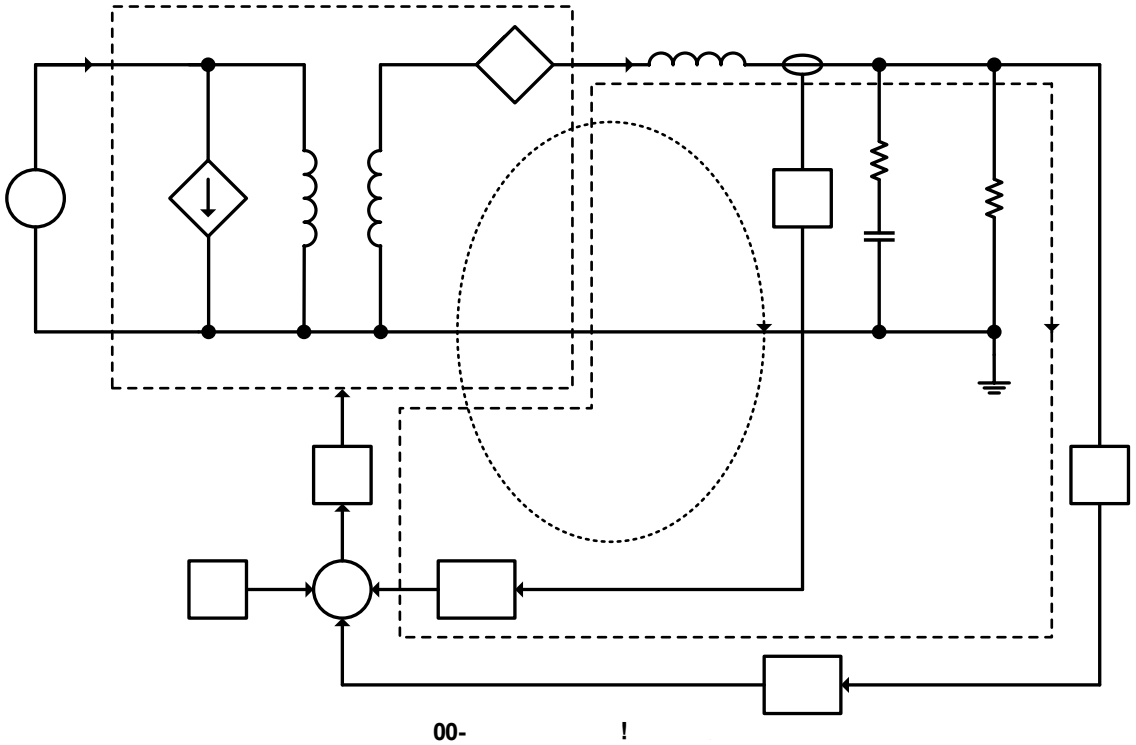
When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses constant frequency peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. The system becomes a single order system. It is much easier to design a type II compensator (Figure 12) to stabilize the loop than in case of a voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 11 shows the small signal model of the synchronous buck regulator.



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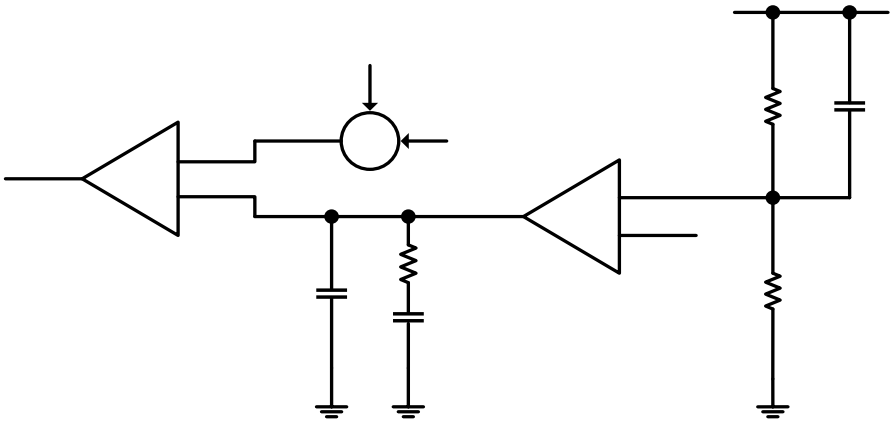
Where:

$T_v(S)$ is the voltage loop
$T_i(S)$ is the current loop
$K(S)$ is the voltage sense gain
$-A_v(S)$ is the feedback compensation gain
$H_e(S)$ is the current sampling function
F_m is the PWM comparator gain
V_{in} is the DC input voltage
D is the duty cycle
R_c is the ESR of the output capacitor, COUT
R_o is the output load resistance$\hat{v}_{in}$ is the AC small-signal input voltage
$\hat{i}_{in}$ is the AC small-signal input current
$\hat{d}$ is the modulation of the duty cycle
$\hat{i}_L$ is the AC small signal of the inductor current
$\hat{v}_o$ is the AC small signal of output voltage
$\hat{v}_{comp}$ is the AC small signal voltage of the compensation network



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Transfer function of Figure 12 is expressed in the following equation,

The goal of loop compensation design is to achieve:

High DC Gain
Gain Margin less than -10dB
Phase Margin greater than 45°
Loop Bandwidth Crossover Frequency (f_c) less than 80kHz (10% of f_{sw})

The loop gain at crossover frequency of fc has a unity gain. Therefore, the compensator resistance R3 is determined by equation below. A recommended rule of thumb is to set the crossover frequency to be approximately 1/5 to 1/10 of switching frequency.

(13)

Where

gm=0.3mS,
Rt=0.2V/A
VFB=0.8V,
fc is the desired crossover frequency
Vout is the output voltage
Co is the effective output capacitance.

Be cautioned that most ceramic will degrade with voltage stress or temperature extremes.

The compensator capacitor C6 and C7 are then equal to:

(14)

Where :

Io is the output load current
Rc is the ESR equivalent of the Co
Fs is the switching frequency. In most cases, C7 can omit.

An optional zero, z2, can boost the phase margin but it can also increase the gain crossover. Place this zero at 2 to 5 times the fc. Then C4 is equal to:

(15)

1- **(** **,** **(** **,**

					2k				

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Vin=12V, Vout=5V,

Figure 25 and Figure 26 are the recommended PCB layout of SCT9433 with or without external compensation network.

1. The SCT9433 works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias under both the thermally exposed GND pad and GND plane for heat dissipation to all the GND layers.
8. Add as many vias under both the thermally exposed VIN pad and VIN plane for heat dissipation to all the VIN layers.

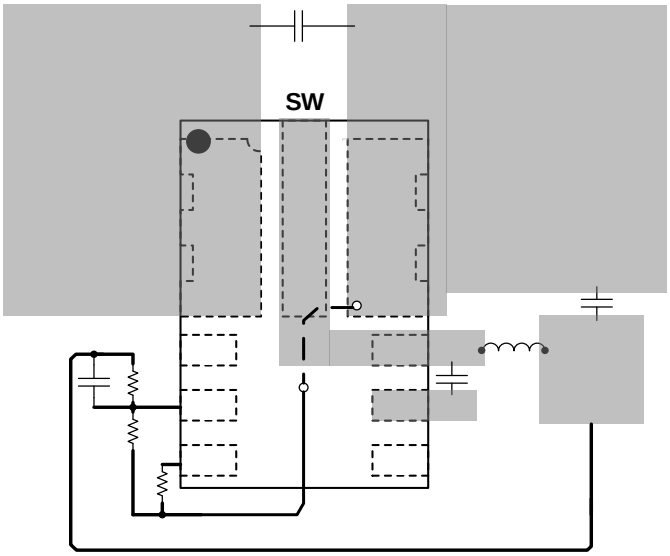

Figure 25. PCB Layout Example for application with internal compensation

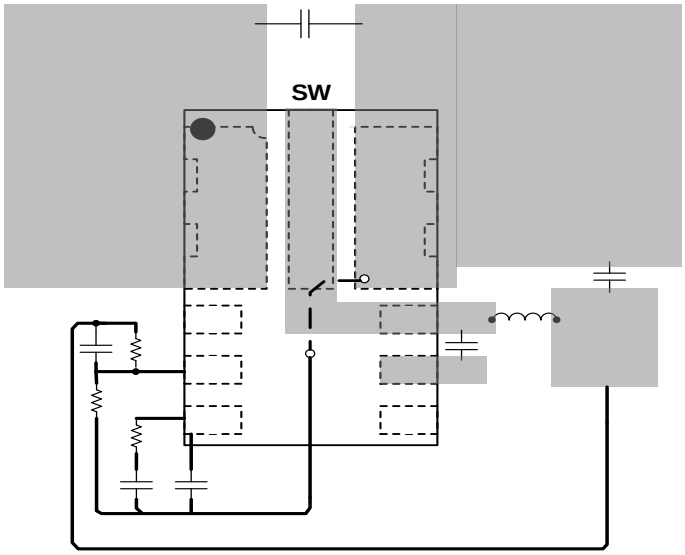

Figure 26. PCB Layout Example for application with external compensation

FCQFN-9L (2*3) Package Outline Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.2	0.25	0.3
b2	0.25	0.3	0.35
D	2 BSC		
E	3 BSC		
e	0.45 BSC		
e1	0.475 BSC		
e2	0.575 BSC		
e3	0.1 BSC		
L	0.35	0.40	0.45
L1	0.55	0.6	0.65
L2	1.475	1.525	1.575
L3	0.15 REF		
aaa	0.1		
ccc	0.1		
eee	0.05		
bbb	0.1		

1v

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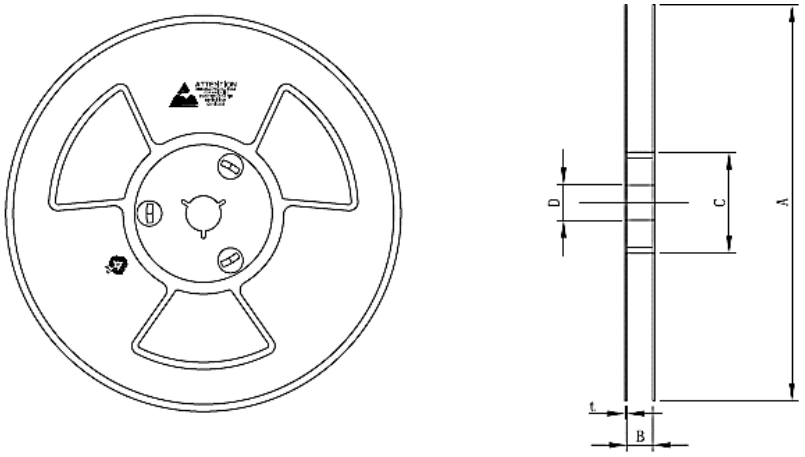
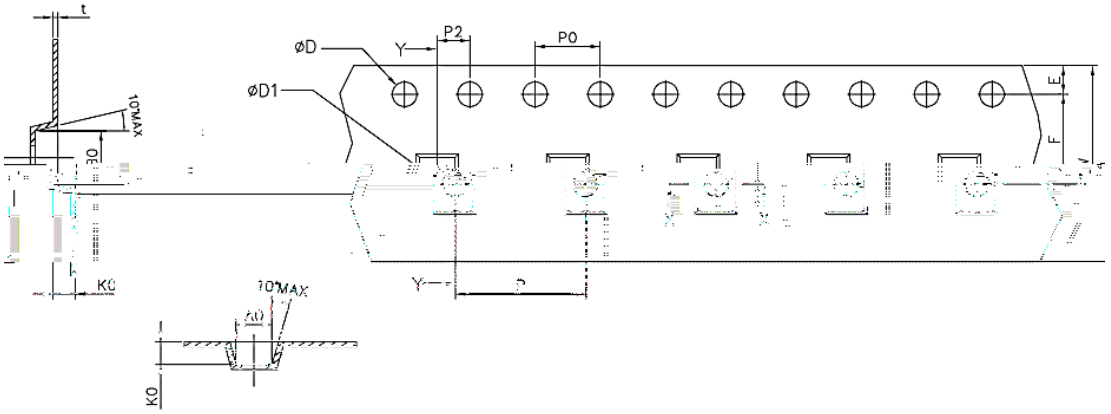
Orderable Device	Package Type	Pins	SPQ
SCT9433FSAR	QFN 2mmx3mm	9	5000



! %	! !		
	!	%!	!
	328	329	330
	11.80	12.80	13.80
	99	100	101
	13.00	13.30	13.60
	1.70	2.00	2.30



! %	! !		
	!	%!	!
	1.65	1.75	1.85
	5.45	5.50	5.55
1	1.95	2.00	2.05
		1.50	1.60
0		1.50	1.75
/	3.90	4.00	4.10
	11.90	12.00	12.30
	7.90	8.00	8.10
/	2.10	2.20	2.30
/	3.20	3.30	3.40
/	1.04	1.14	1.24
	0.23	0.25	0.27

