3.8V-40V Vin, 3.5A, High Efficiency Synchronous Step-down DCDC Converte

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

Revision 1.1: Update thermal information in page 3

DEVICE ORDER INFORMATION

SCT2433DSTE	433D	8-Lead Plastic ESOP

1) For Tape & Reel, Add Suffix R (e.g. SCT2433DSTER)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

VIN, EN	-0.3	42	V
BOOT	-0.3	48	V
SW	-0		

PIN CONFIGURATION

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ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		3.8		40	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		3.5 400		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1		μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		290		μA
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		80		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			50		mΩ
V_{REF}	Reference voltage of FB			0.8		V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		4.25	5	5.75	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold			5.5		A
T_{HIC_W}	Over current protection hiccup wait time			512		cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		cycles
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1.5		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		uA
T_{ss}	Internal soft start time			2		ms
F_{SW}	Switching frequency		510	570	630	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		100		ns
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.36 300		V mV
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		170 25		°C °C

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TYPICAL CHARACTERISTICS

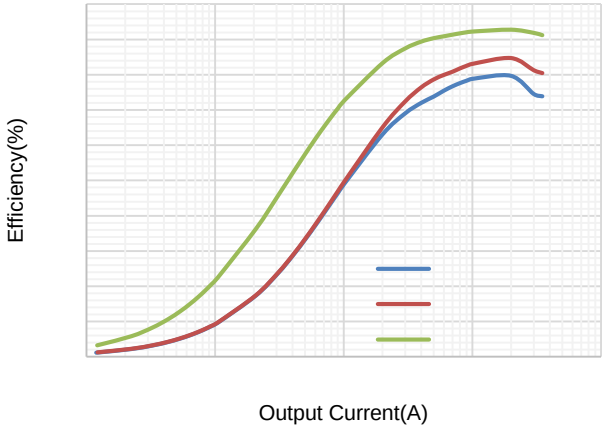

Figure 2. Efficiency vs Load Current, Vin=36V

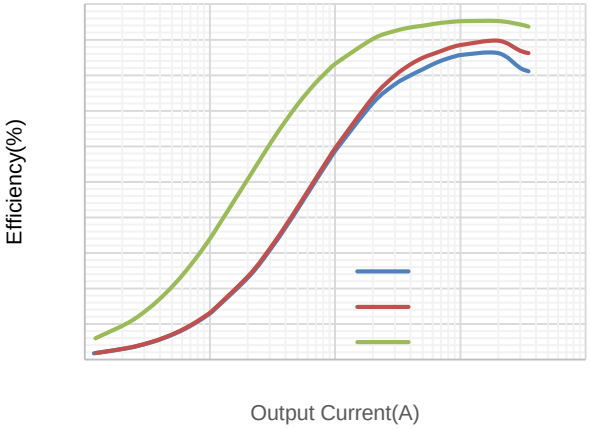

Figure 3. Efficiency vs Load Current, Vin=24V

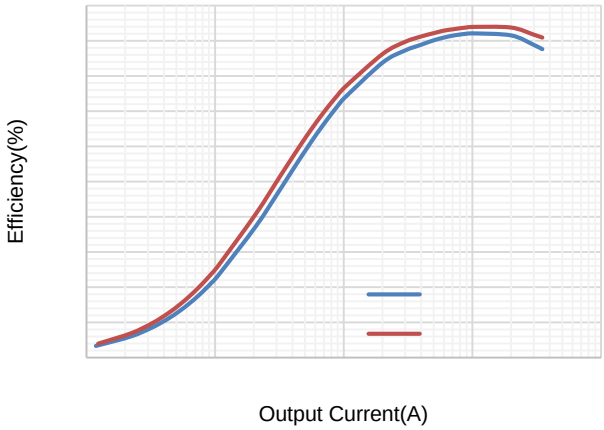

Figure 4. Efficiency vs Load Current, Vin=12V

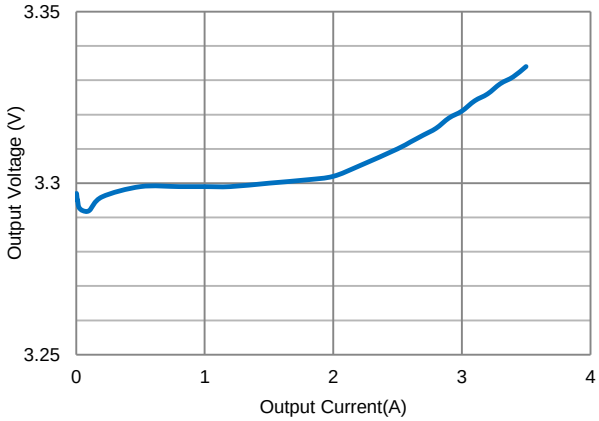

Figure 5. Load Regulation (Vin =12V, Vout=3.3V)

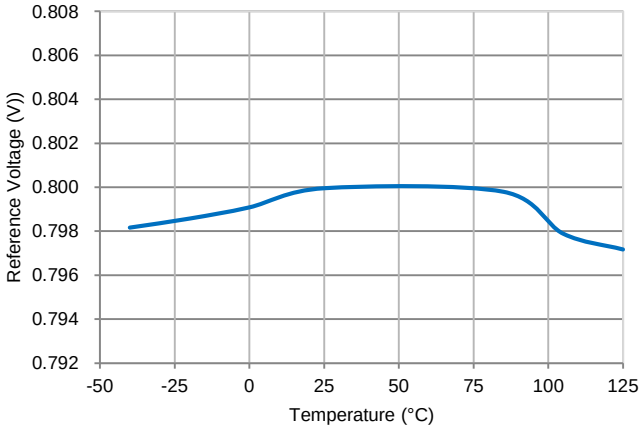

Figure 6 Reference Voltage vs Temperature

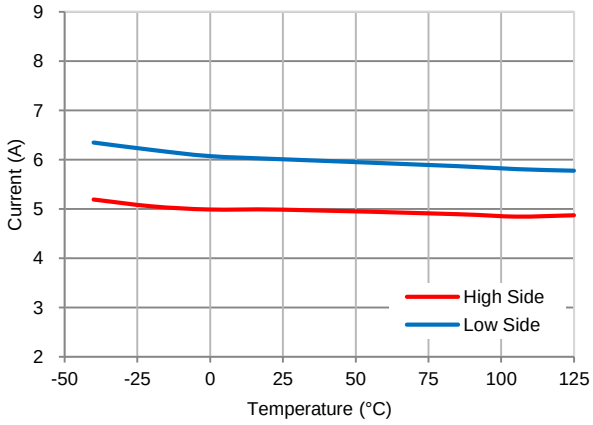

Figure 7. Peak Current Limit vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

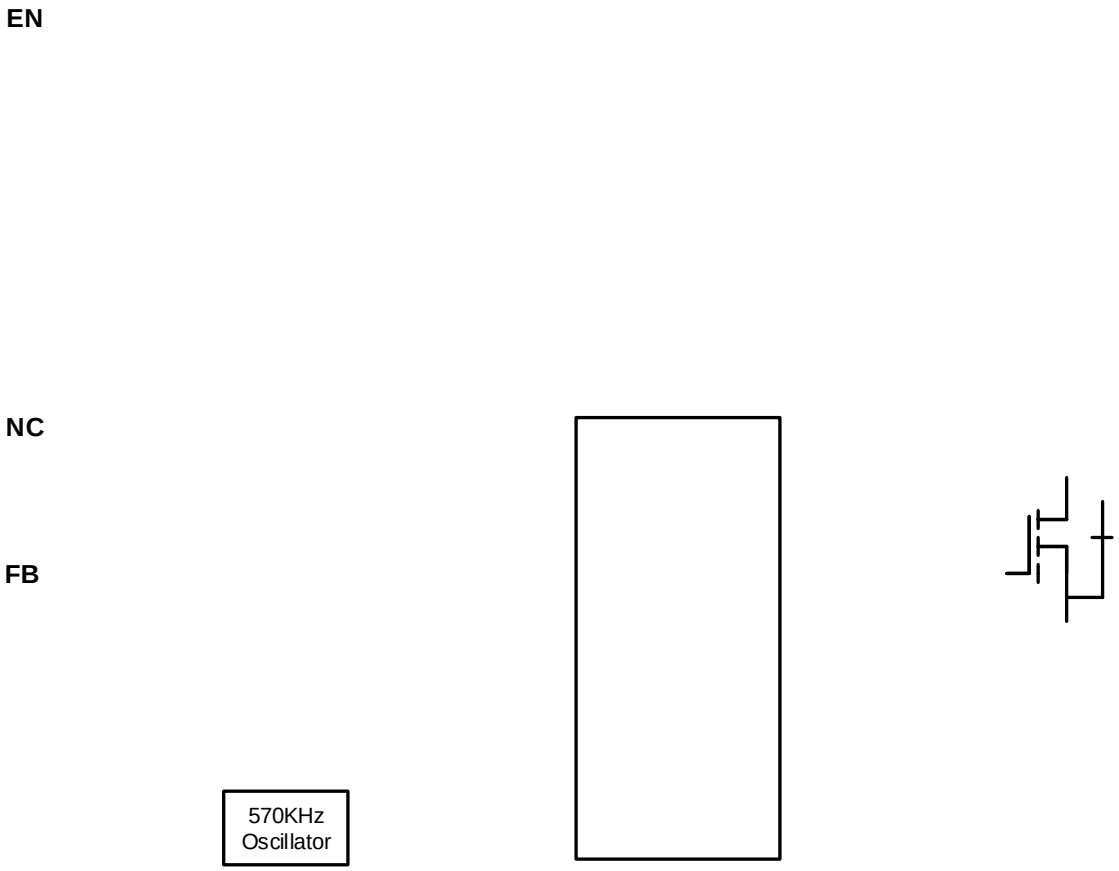

Figure 8. Functional Block Diagram

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OPERATION

The SCT2433D is a 3.8V-40V input, 3.5A output, EMI friendly synchronous buck converter with built-in 80mΩ Rdson high-side and 50mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control with internal compensation to regulate output voltage, providing excellent line and load transient response and make free the frequency compensation design. The SCT2433D features 2ms internal soft-start time to avoid large inrush current and output voltage overshoot during startup and the switching frequency is 570kHz fixed. The device also supports monolithic startup with pre-biased output condition.

The SCT2433D has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2433D implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered the selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2433D full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

The SCT2433D employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2433D is enabled when the VIN pin voltage rises about 3.5V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$M \quad 22 \quad 2 \quad \frac{I\,2}{I} \quad 26 \quad I\,2 \qquad (1)$$

$$M \quad 22 \quad 2 \quad \frac{I\,2}{I} \quad 66 \quad I\,2 \qquad (2)$$

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

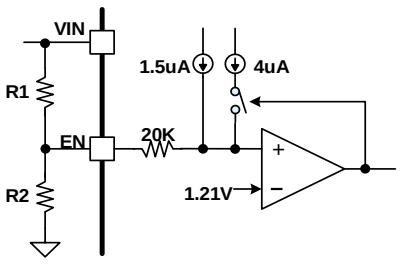

Figure 9. System UVLO by enable divide

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The SCT2433D regulates the internal reference voltage at 0.8V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better

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The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2433D implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current runningent

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The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 4 to calculate R5.

—— 2 (4)

where:

V_{REF} is the feedback reference voltage, typical 0.8V

1.8 V	12.7 KΩ	10.2 KΩ
2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.7V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.64 V (stop or disable). Use Equation 5 and Equation 6 to calculate the values 173 kΩ and 42 kΩ of R_1 and R_2 resistors.

M 22 2 — 26 I 6

M 22 2 — 66

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$$\frac{\qquad\qquad\qquad\qquad 2}{\qquad\qquad} \tag{8}$$

Where

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 9 and equation 10.

$$\frac{\qquad}{\qquad\qquad\qquad\qquad} \tag{9}$$

$$\frac{\qquad\qquad\qquad\qquad}{\frac{2}{2}} \tag{10}$$

Where

I_{LPEAK} is the inductor peak current
I_{OUT} is the DC load current
I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2433D can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.2 or 0.3, and the inductor value is calculated to be 5.7uH, the RMS inductor current is 3.51A and the peak inductor current is 4A. The chosen inductor is a WE 744325650, which has a saturation current rating of 10A and a RMS current rating of 8.4A. This also has a typical inductance of 6.5µH at no load and 6 µH at 4A load. The inductor DCR is 12.5 mΩ.

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage usÆ ϵ ⁄ap

high freque rr Ï v Ğ ɹ ϵe it is st Ɛ . .

$$\frac{M}{M} \quad 2 \quad \frac{M}{M} \qquad (11)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

1 6 (12)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$M \quad \frac{M}{M} \quad 2 \quad \frac{M}{M} \qquad (13)$$

For this example, three 4.7μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$M \qquad (14)$$

Where

ΔM is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
$V_{IN}$is the input voltage

Due to capacitor's degrating under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47μF ceramic output capacitors work for most applications.

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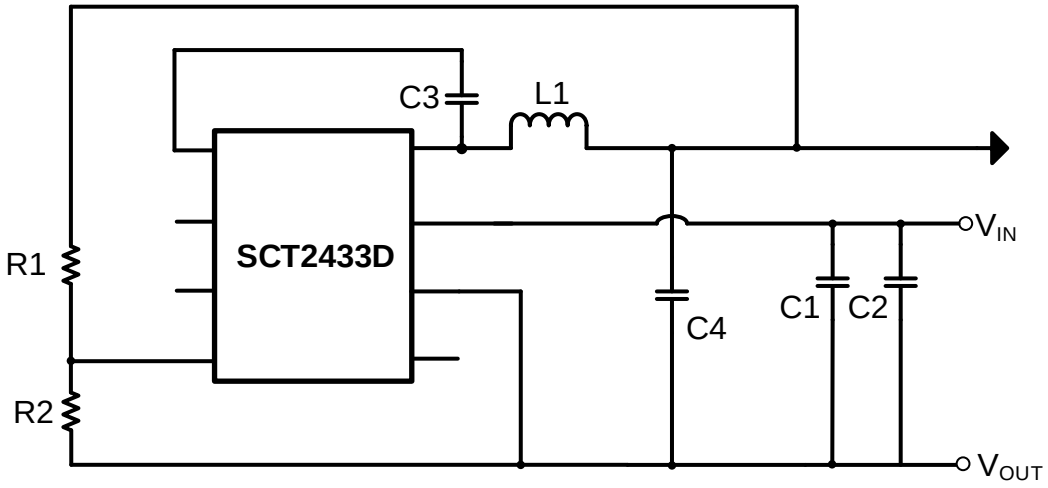
The SCT2433D can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.



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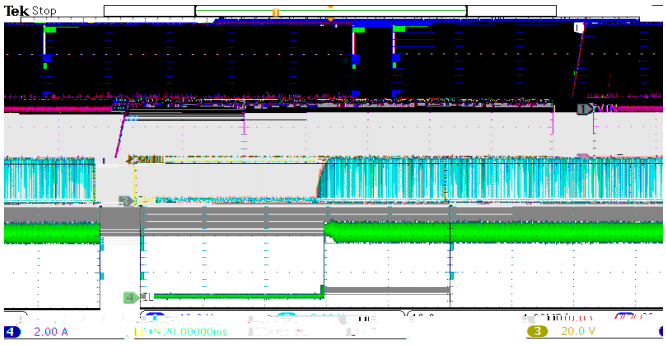

Figure 13. Power up

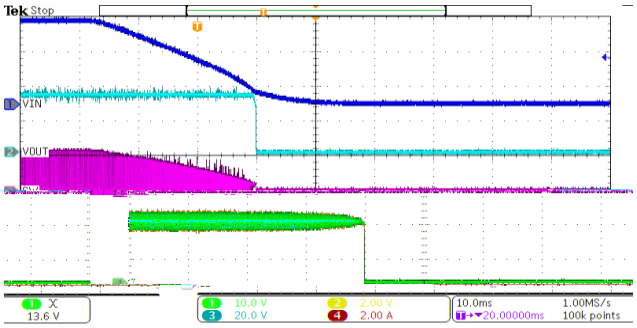

Figure 7. Power down

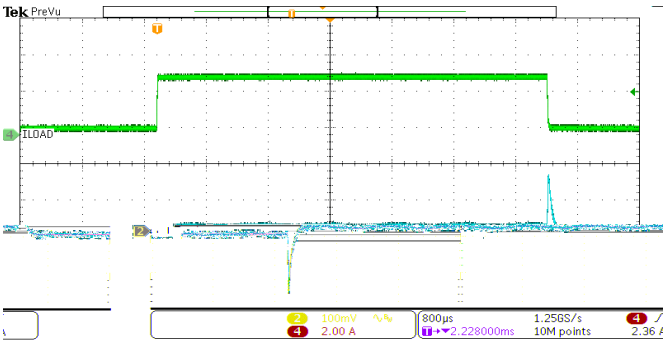

Figure 15. Load Transient (0.35A-3.15A, 250mA/us)

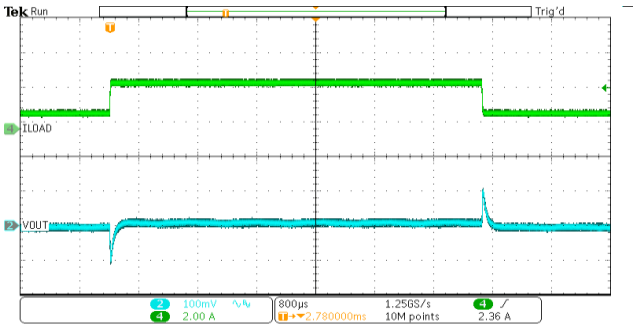

Figure 16. Load Transient (0.875A-2.625A, 250mA/us)

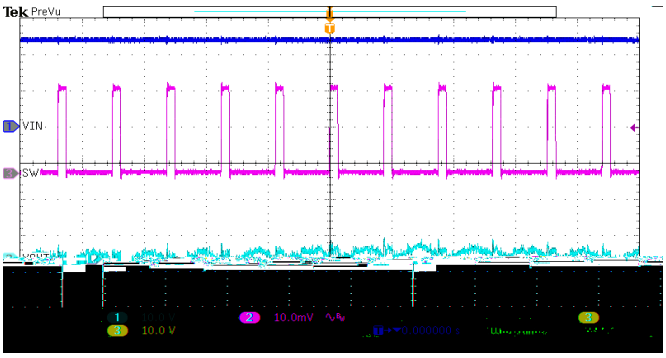

Figure 17. SW and Vout Ripple, (Iout=3.5A)

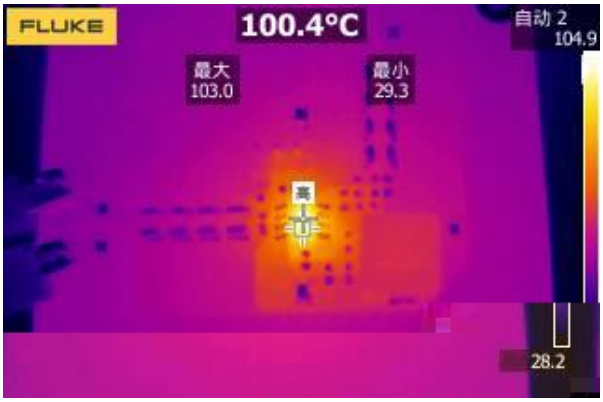

Figure 18. Thermal, 3.3Vout/3.5A

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Proper PCB layout is a critical for SCT2433D's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.

3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

5.

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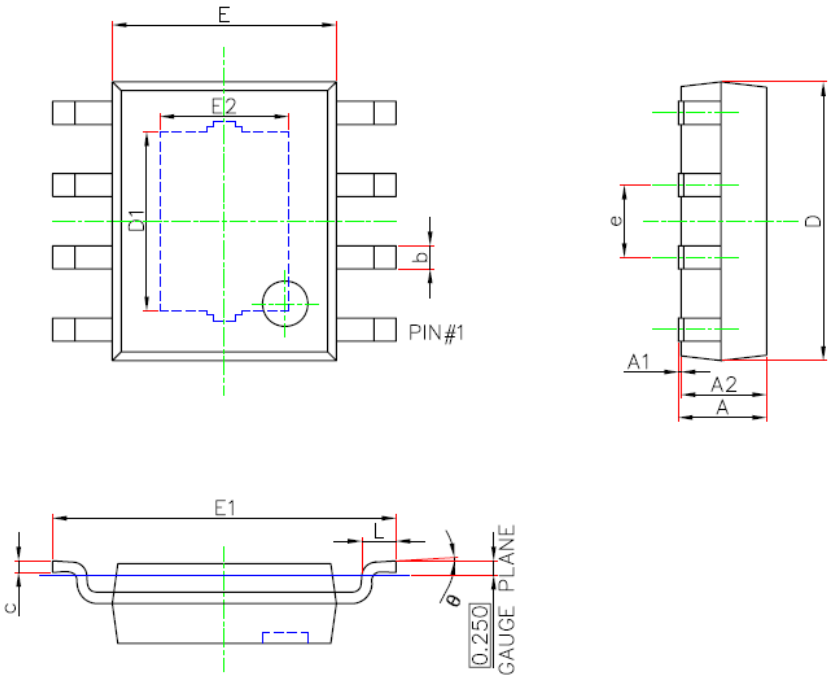
PACKAGE INFORMATION



SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
	0°	8°	0°	8°

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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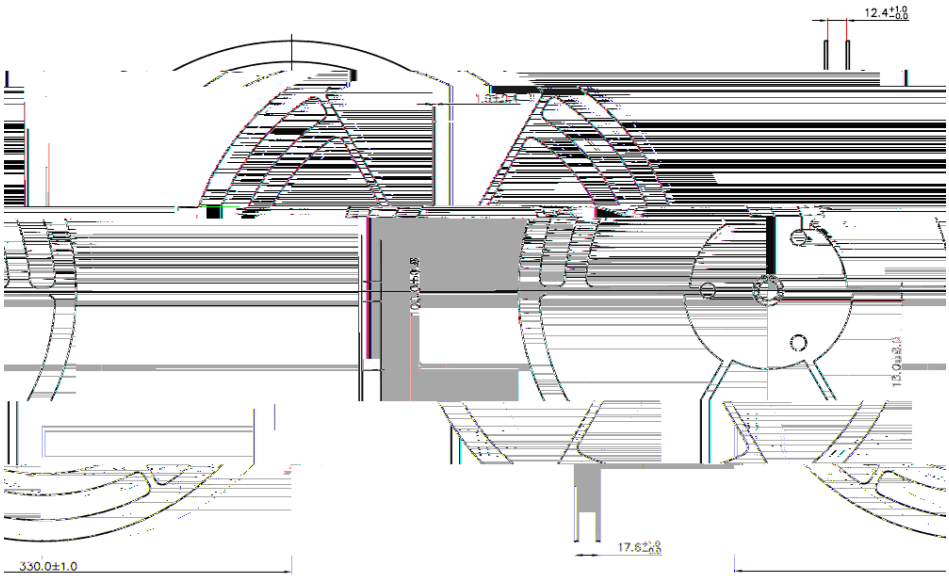
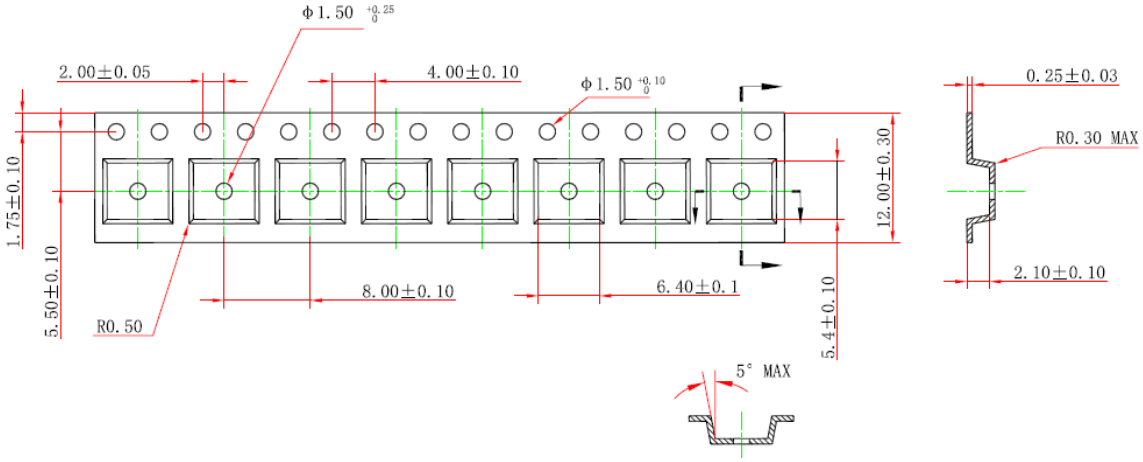
TAPE AND REEL INFORMATION





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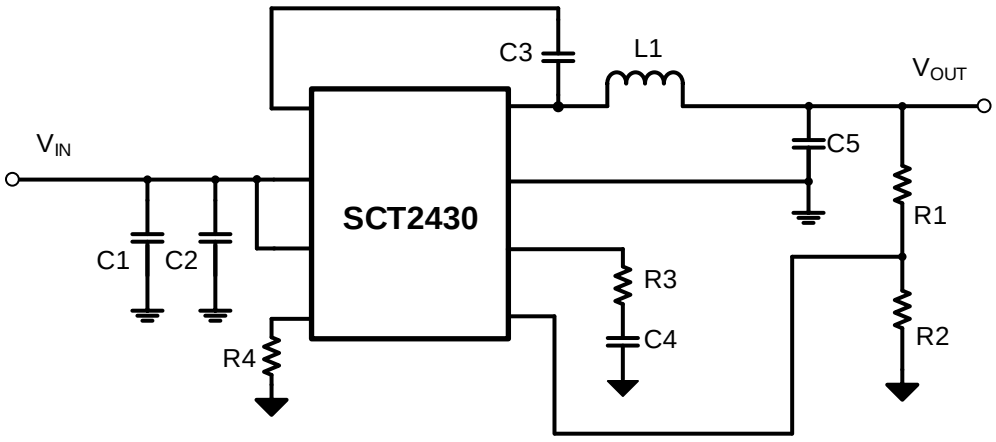
RELATED PARTS

	36V Vin, 5A Synchronous Step-down DCDC Converter with Programmable switching frequency and external synchronous clock	45mΩ / 20mΩ HS/LS MOSFETs Programmable soft start time Freq. = 100KHz- 1.1MHz adjustable Clock synchronization
	36V Vin, 5A Synchronous Step-down DCDC Converter with Adjustable Soft Start Time	45mΩ / 20mΩ HS/LS MOSFETs Programmable soft start time Freq. = 570KHz
	36V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-1.1MHz Programmable Switching Frequency	55mΩ / 30mΩ HS/LS MOSFETs Internal 2ms Soft-time Freq. = 100KHz-1.1MHz adjustable. Clock synchronization
	40V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-2.2MHz Programmable Switching Frequency	80mΩ / 50mΩ HS/LS MOSFETs Internal 2ms Soft-time Freq. = 100KHz-2.2MHz adjustable. Clock synchronization
	36V Vin, 3.5A Synchronous Step-down DCDC Converter with Adjustable Soft Start Time	80mΩ / 50mΩ HS/LS MOSFETs Programmable soft start time Freq. = 570KHz
	40V Vin, 3.5A Synchronous Step-down DCDC Converter with 100KHz-2.2MHz Programmable Switching Frequency, Programmable Soft Start Time and Internal-compensation	80mΩ / 50mΩ HS/LS MOSFETs Programmable soft start time Freq. = 100KHz-2.2MHz adjustable. Clock synchronization Internal Compensation
	40V Vin, 3.5A Synchronous Step-down DCDC Converter	80mΩ / 50mΩ HS/LS MOSFETs Internal 2ms Soft-time Freq. = 570kHz Fix. Clock synchronization



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